Data Sheet
TI DN 2506020 REV D
April, 2005

DMD Discovery™ 1100 DRC (DAD Reset Controller)

This document covers the functionality of the Discovery 1100 DRC (DAD Reset Controller). The Discovery 1100 DRC provides the DMD mirror reset and timing information to the TI DAD1000 DMD Power and Reset Driver.

Revisions		
Rev	Descriptions	Date
717-0040-002 A	Initial release	10/15/03
717-0040-002 B	Complete rewrite with more detailed design information	10/23/04
717-0040-002 C	Corrected timing and mechanical information	2/16/04
717-0040-002 D	Corrected typographical error	2/29/04
TI 2506020 A	Changed to TI drawing number system Corrected pins 84 & 85 on Figure 7	8/13/04
TI 2506020 B	Changed reset active timing in Table 8	10/4/04
TI 2506020 C	Modified Figure 5, typical load and reset sequence on a single block with mirror settling	1/18/05
TI 2506020 D	Added external reset documentation, Section 2.6 Added POR/ descriptions to Figures 3 & 7, Table 1, and Sections 2.2 & 3.10, Table 9	4/7/05

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1 Overview

This document covers the functionality of the Discovery 1100 DRC (DAD Reset Controller). The Discovery 1100 DRC provides the DMD mirror reset and timing information to the TI DAD1000 DMD Power and Reset Driver.

Shown below are two simplified block diagrams (Figure 1, Figure 2) showing the use of the DRC with and without the use of the USB interface.

The block diagram in Figure 1 is a typical system using both high-speed (HS) and USB interfaces. The end-user may control the DMD from either the USB or HS interface. When the USB Interface Controller is used, DMD mirror resets are initiated through the USB interface and passed to the DRC through the USB support components. The DRC provides the reset logic required for the DAD1000 to drive the DMD mirror reset inputs.

The six components shown are:

DMD 0.7XGA 12^{o} DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver for DMD
Cypress FX2 – 2.0 USB controller
Discovery 1100 USBIFC (USB Interface Controller) – provides interface between USB and DMD Components
Discovery 1100 DRC (DAD RESET Controller) – provides reset interface to DAD and DMD
Discovery 1100 HSC (HS Controller) – provides high-speed clock control and command interface

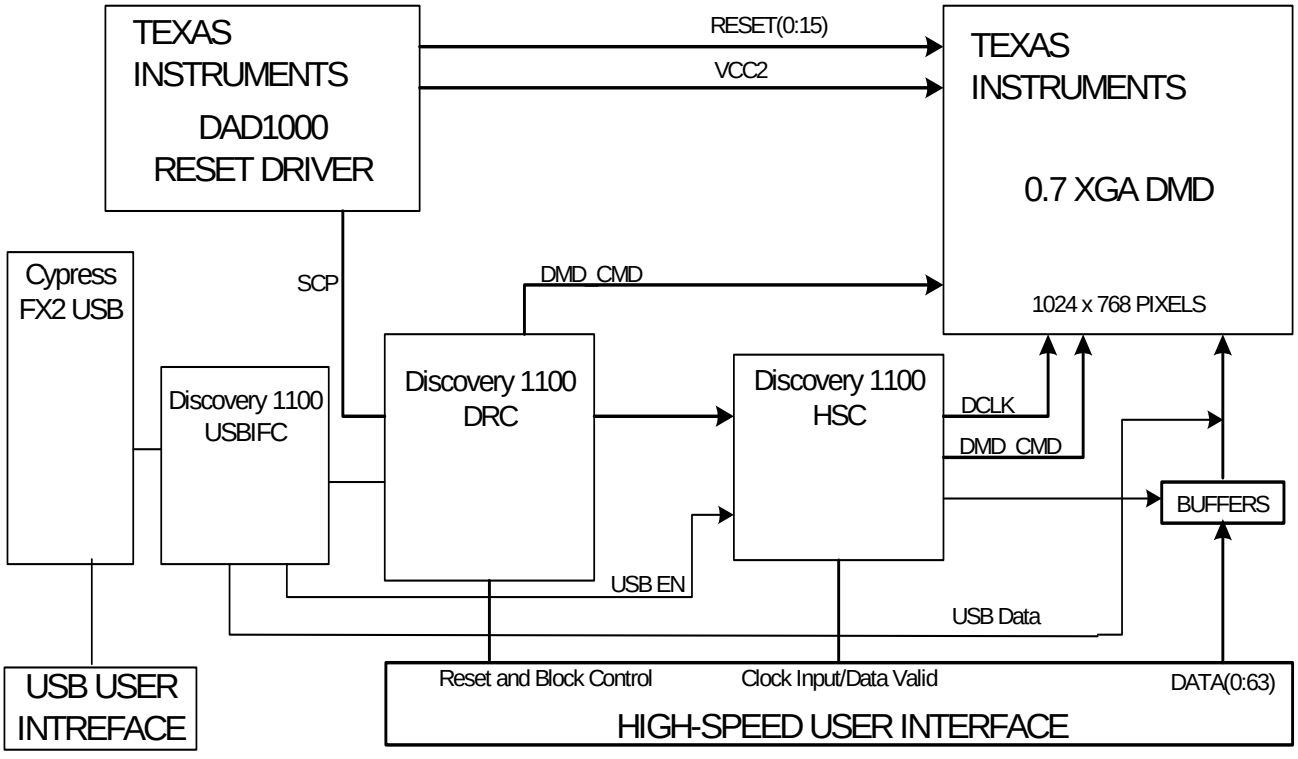


Figure 1 Discovery Block Diagram with USB

The second block diagram shown in Figure 2 shows a typical system with high-speed only interface. In this system, the DMD mirror reset commands are initiated and passed directly to the DRC through the High-Speed interface.

The four components shown are:

DMD 0.7XGA 12° DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver for DMD
Discovery 1100 DRC (DAD RESET Controller) – provides reset interface to DAD and DMD
Discovery 1100 HSC (HS Controller) – provides high-speed clock control and command interface

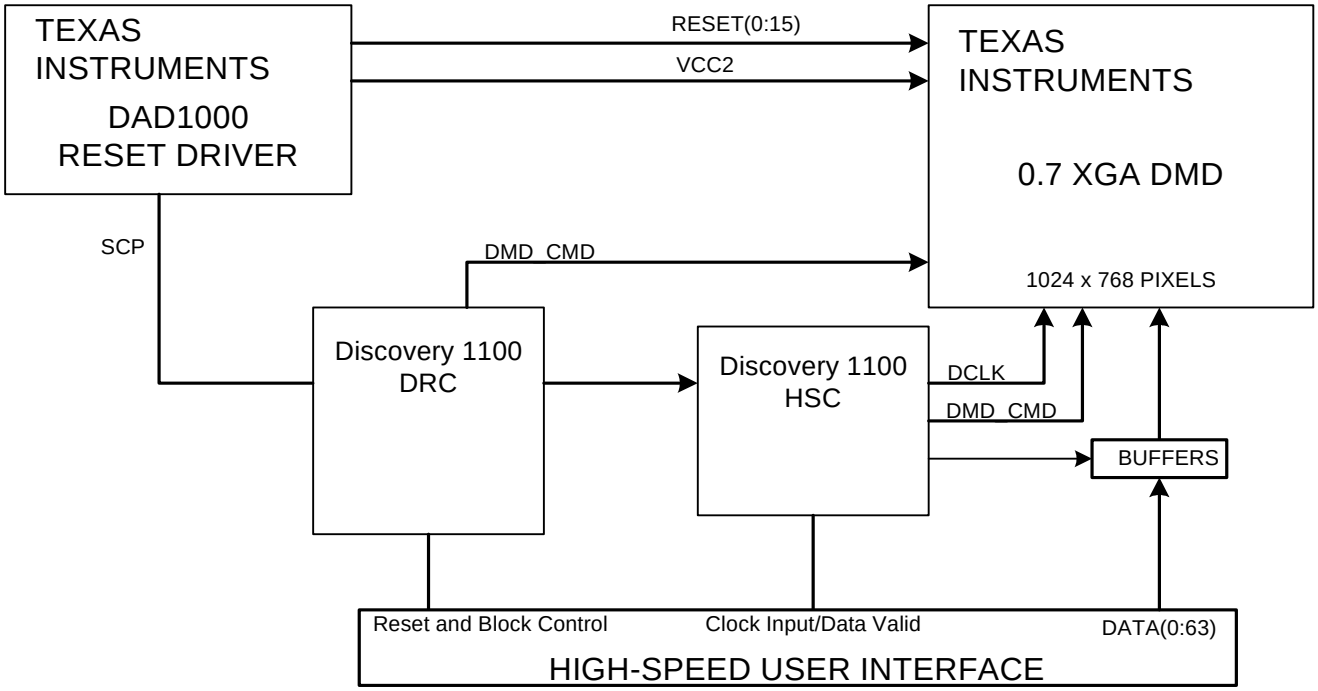


Figure 2 Discovery Block Diagram without USB

2 Functional Description

The internal structure of the DRC is divided into six major blocks. See block diagram below –

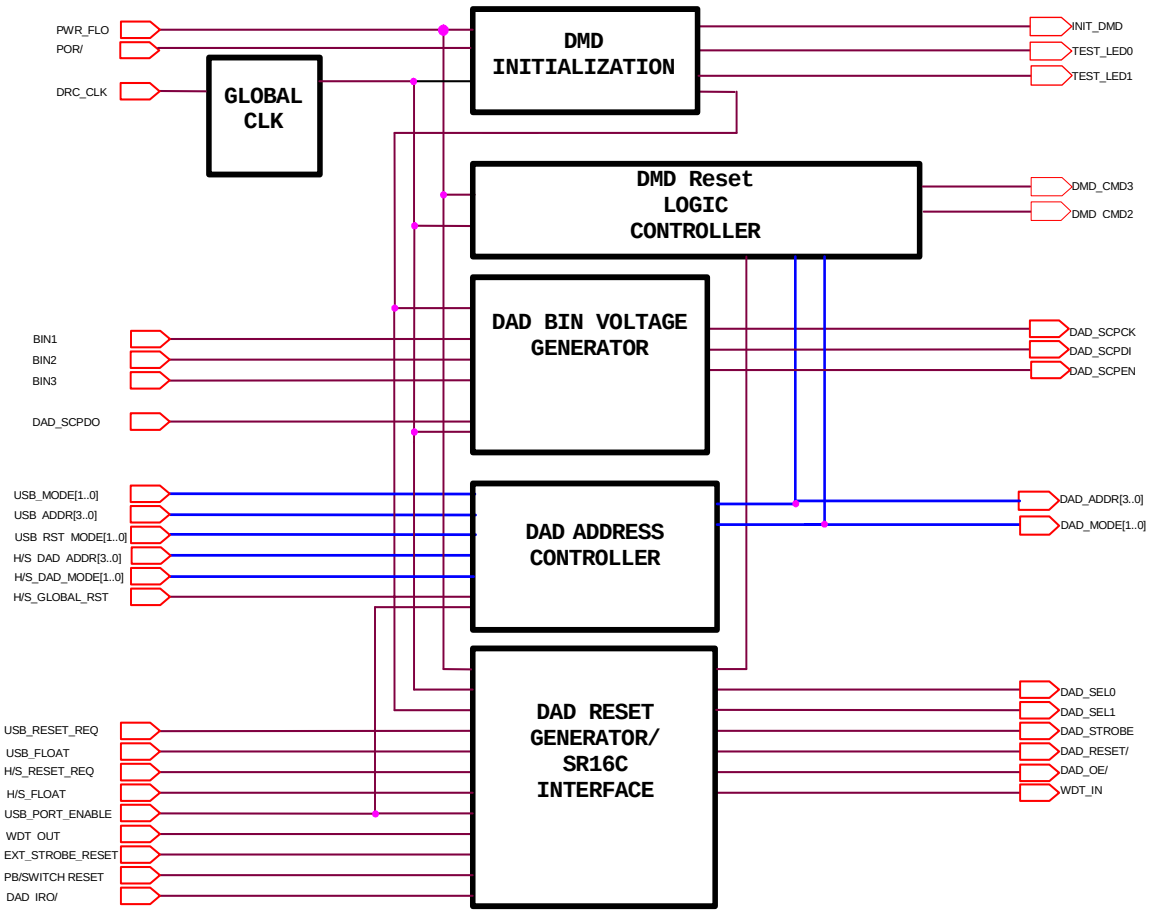


Figure 3 DRC Functional Block Diagram

2.1 Global Clock

The 60MHZ on board clock is used as a global clock that provides clocking for all internal timing and clocking.

2.2 DMD Initialization

After all DRC registers are cleared on power up, the DMD Initialization block generates commands to set DAD1000 bin voltages and to reset the DMD. INIT_DMD is initally set to a logic low, which begins initialization of the DAD1000 and the Logic Controller block, and finally the DMD is reset. After the initialization is complete, INIT_DMD goes to logic high.

2.3 DMD Reset Logic Controller

This block generates mirror reset control signals directly to the DMD. These signals are used with the DAD1000 reset signals connected to the DMD to place mirrors in the desired position.

2.4 DAD Voltage Bin Generator

This block generates DMD mirror reset bin voltage information for DAD1000.

2.5 DAD Address Controller

This block selects DMD mirror reset group address bits from either the USB or high-speed interface.

2.6 DAD Reset Generator

This block generates DAD1000 DMD mirror reset or float signals initiated either from the USB or high-speed interface. When in USB mode a reset may be triggered through the USB_RESET_REQ, EXT_STROBE_RESET/ or PB/SWITCH_RESET/ pins.

3 PIN FUNCTIONAL DESCRIPTION

The DRC provides all of the logic necessary to control the DMD and DAD1000 devices in conjunction with the HSC and the USB. Table 1 list functions that the designer has access or control of in design applications. Table 9 lists all signal and connections required when used with other chipset components.

Table 1 User I/O Pin Descriptions

Pin Name	Description	I/O
HS_RESET_ACTIVE	Indicates Reset is Active	O
HS_RESET_REQ	Reset request from HS port	I
HS_FLOAT	Float request from HS port	I
HS_GLOBAL_RST	HS Global Reset Request. Overrides the BLOCK or MODE bit addresses	I
HS_DADMODE [0:1]	DAD Mode Select from HS port	I
HS_ADDR [0:3]	DAD Reset Block address select from HS port	I
WDT_OUT	Watchdog timer output. Initiates DMD mirror reset if elapsed time on timer has expired	I
WDT_IN	Watchdog Timer input	O
POR/	Power-on reset clears all DRC registers	I
INIT_DMD	Indicates DMD is in Initialization	O
USB_PORT_ENABLE	Selects between USB and high-speed interface reset commands. HIGH selects high-speed interface. A 1K ohm pull-up should be placed on this line at the input of this component,	I
DAD_IRQ/	Not currently used, input from DAD. Should be connected as indicated in Table 9 for possible future use.	I
BIN (1:3)	Used to set voltage bins in DAD1000. Currently must all be pulled high for Discovery DMD to 3.3V. Suggest using jumper or switches to provide the ability to set these signals low if required by TI in the future for Discovery DMDs. This is a factory specified setting. Setting to other than factory specified settings could lead to undesired operation.	I
TEST_LED0	Indicates when initialization of DMD is complete. Tracks with INIT-DMD signal	O
TEST_LED1	Heartbeat to indicate state machines are running	O
PWR_FLOAT/	On power-down floats mirrors on DMD.	I
DRC_CLK	Used as global clock for controller. Must be 60 MHZ.	I
DAD_OE/	This signal provides a low to enable the DAD reset outputs	O
OE1/	Enables Outputs of DRC, should be tied to ground.	I
VCCINT	VCC 2.5V	P
VCCIO	VCC 3.3V	P
GNDINT	Ground	P
GNDIO	Ground	P

3.1 HS_RESET_REQ and HS_RESET_ACTIVE

The HS_RESET_REQ starts the reset sequence and the HS_RESET_ACTIVE indicates when the reset logic is available to start the next reset. Refer to Figure 4 for a typical reset sequence. It should be noted that no other resets should be initiated while the HS_RESET_ACTIVE signal is active. While a reset function is active (HIGH), this signal indicates that the reset is in process. This signal goes active (high) about 100ns after HS_RESET_REQ goes active (high) and will stay high about 6.2us. While HS_RESET_REQ is high, and for 4-12us after, the data for the block(s) being reset should not be changed to allow for the settling required for the mirrors to become stable. The ability to load new data into other blocks that have not been recently reset is not affected. Figure 5 shows a single block load, reset, andreload sequence with the light gray areas indicating mirror-settling time. The minimum mirror settle time is determined by what DMD mirror design is used. Although a minimum of 12us was required for older, XB DMDs, the mirror settle time for FTP DMDs is 4us. Please see DN 2503884 for FTP and XB DMD part number information.

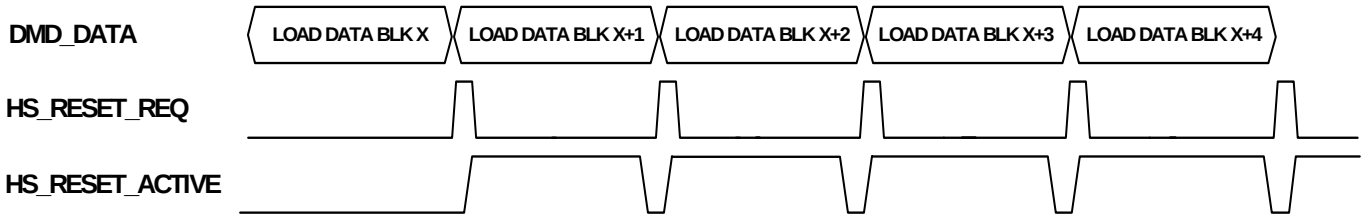


Figure 4 Typical Phased Reset Sequence

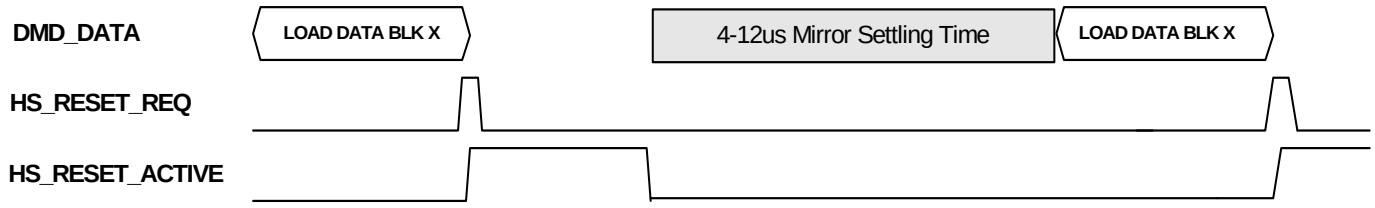


Figure 5 Typical Load and Reset Sequence on a single block with Mirror settling

3.2 Reset Block Selects (HS_ADDR [0:3] and HS_DADMODE [0:1])

These bits allow the selection of which block or groups of blocks will be reset. See Table 2 for a list of combinations. Access to these signals allow for phased reset operation. There can be up to 3 mirror groups in reset at one time.

Table 2 Reset Groups

HS_DAD_ MODE1	HS_DAD_ MODE0	HS_ ADDR3	HS_ ADDR2	HS_ ADDR1	HS_ ADDR0	Selected Reset Group
0	0	0	0	0	0	**00**
0	0	0	0	0	1	**01**
0	0	0	0	1	0	**02**
0	0	0	0	1	1	**03**
0	0	0	1	0	0	**04**
0	0	0	1	0	1	**05**
0	0	0	1	1	0	**06**
0	0	0	1	1	1	**07**
0	0	1	0	0	0	**08**
0	0	1	0	0	1	**09**
0	0	1	0	1	0	**10**
0	0	1	0	1	1	**11**
0	0	1	1	0	0	**12**
0	0	1	1	0	1	**13**
0	0	1	1	1	0	**14**
0	0	1	1	1	1	**15**
0	1	0	0	0	X	**00-01**
0	1	0	0	1	X	**02-03**
0	1	0	1	0	X	**04-05**
0	1	0	1	1	X	**06-07**
0	1	1	0	0	X	**08-09**
0	1	1	0	1	X	**10-11**
0	1	1	1	0	X	**12-13**
0	1	1	1	1	X	**14-15**
1	0	0	0	X	X	**00-03**
1	0	0	1	X	X	**04-07**
1	0	1	0	X	X	**08-11**
1	0	1	1	X	X	**12-15**
1	1	X	X	X	X	**00-15**

3.3 H/S_FLOAT

This signal should be used to place the mirrors in a float position not landed to either ”on” or “off” position. Once the mirrors are placed in the float position, they will stay in the float position until the mirrors are reset with a HS_RESET_REQ. See Figure 11 for timing details.

3.4 H/S_GLOBAL_RST

If the global reset flag is set, the reset block select inputs are ignored, and all 16 reset blocks are reset simultaneously when HS_GLOBAL_RST is asserted. Refer to Figure 10 for timing information.

3.5 WDT_OUT

When this signal goes low, a DMD mirror reset is generated. It's intended to be used as an input from a watchdog timer so that the mirrors do not stay in a set position for extended periods. See the Discovery DMD Customer Data Sheet for information regarding the length of time the mirrors are allowed to stay set in the same position.

3.6 WDT_IN

This signal outputs a positive pulse each time the DRC receives a reset request. This pulse can be used to reset an external watchdog timer.

3.7 BIN [1:3]

These bits control the reset voltages to the DMD. Currently all Discovery DMDs require these bits to be pulled high. Changing these value can lead to unreliable operation.

3.8 TEST_LED0

This output can be used to drive an LED to Indicate when initialization of DMD is complete. The DMD is considered initialized when all of the required setup is done and the mirrors are cycled and put into a known state. This signal is active low while initialization is in process, and then goes high when initialization is complete.

3.9 TEST_LED1

This is a "heartbeat" output that can be used to drive an LED to indicate that system is initialized and operational.

3.10 POR/

This input must transition from low to high at least 10ms after power-up in order to initialize the DRC registers.

3.11 INIT_DMD

This signal indicates that the DRC is initializing the DAD1000 by setting all internal registers to their correct states, and then initiating a DMD mirror reset. When this signal goes high, the DRC has completed initialization.

3.12 USB_PORT_ENABLE

When this signal is low, the DRC is controlled by the inputs from the USB Interface Controller. When high it is controlled by the HS interface signals.

3.13 PWR_FLOAT/

This signal is to be used to float (place mirrors in a flat condition) the mirrors when power is removed. The signal should be high for normal operation. An external voltage-monitoring device should be used to detect when the 5-volt supply drops below 3.6 volt, and then drive this signal low.

3.14 DRC_CLK

This clock provides the base timing for the DRC. It must be 60MHZ or the DMD will not operate reliably.

3.15 DAD_OE/

In this part, this signal provides a low to enable the DAD reset outputs. Refer to the DAD1000 CDS for a more detailed description of the input into the DAD.

4 Layout Guidelines

4.1 Overview

The Discovery DDC1100 component set provides a highly integrated, high performance DMD solution that enables designers to create small size, high data rate products. The component set, when implemented with the reference material provided, provides all the electronics required to drive and control the DMD sub system on a small PWB depending on configuration

The majority of the circuitry in the DDC1100 reference design is high-speed digital. High-speed digital circuitry includes a 64 bit input data interface, and an HRC (high-speed controller) to DMD interface. Proper layout of the high-speed digital and analog circuits is critical to insure a working and robust design.

Items covered in this section deal mainly with the DRC. See the DDC1100 Controller Board TRM for a system overview.

4.2 High Speed Signals

In addition to the oscillator circuit, most signals are either 60 MHz or 120 MHz. High-speed design techniques should be used with these signals. It is recommended that series termination resistors be placed close to these output pins and trace length of these signal be keep short and as close to the same length as possible. It is suggested that high-speed signals maintain a trace impedance of 50 ohms.

4.3 Oscillators

The DRC utilizes oscillators for the DAD interface. PSI recommends PI filters on the power entry to the oscillators as an EMI precaution. The PI filter capacitor on the oscillator side should be located as close to the oscillator's supply pin as possible. The series termination resistor on the oscillator clock output should be located close to the output pin on the oscillator. Having a surface ground plane under the oscillator package can reduce EMI radiation. The surface ground plane should be tied to the internal ground planes with multiple vias.

4.4 DC Supply Voltages

The DRC electronics requires DC supply voltages of 2.5V, 3.3V. PSI recommends filtering these supply voltages with PI filters. The PI filters should be located at the power entry to the PWB. Trace widths for the supply voltages and ground connections should be sized based on current and desired temperature rise in accordance with a standard such as IPC-2221.

4.5 Decoupling Capacitors

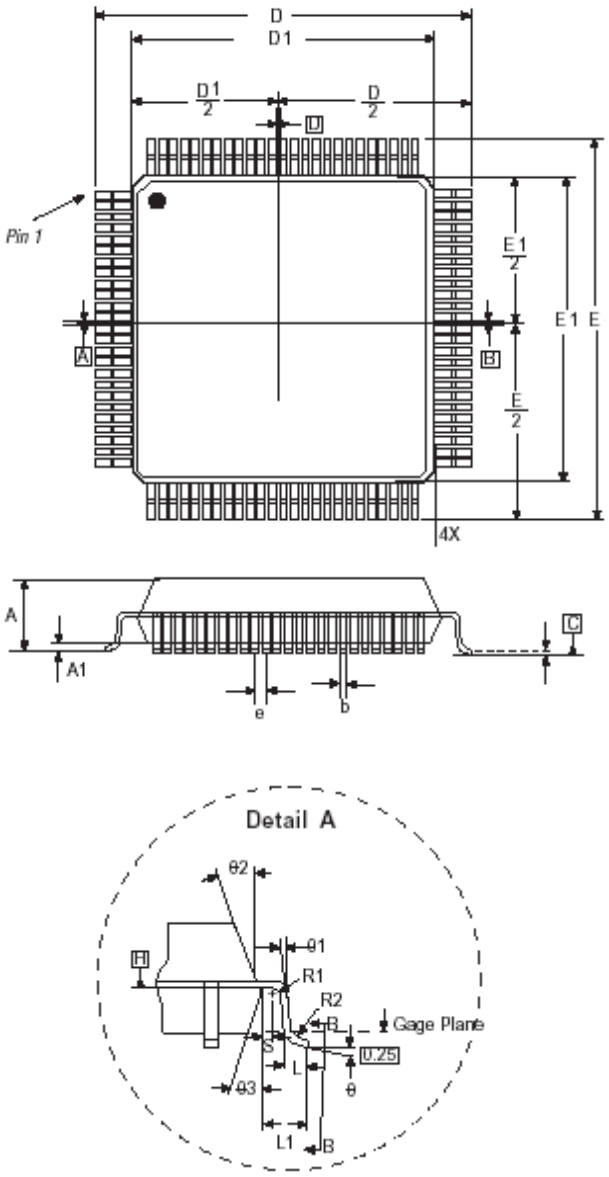
Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component.

- The supply voltage pin of the capacitor should be located very close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1". Otherwise the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1" to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

5 DEVICE PACKAGING INFORMATION

5.1 Pin Diagram

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min	**Nom.**	**Max**
A	-	-	1.27
A1	0.05	-	0.15
b	0.17	0.22	0.27
D	15.80	-	16.20
D1	13.50	-	14.50
E	15.80	-	16.20
E1	13.50	-	14.50
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°		13°
θ3	11°		13°
C	0.09	-	0.20
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
e	0.50 BSC		
N	100		



Notes:

1. **All dimensions and tolerances conform to ANSI Y14.5 – 1994**
2. **Controlling dimensions: millimeters.**
3. **JEDEC reference MS-029 option FA-1.**

Figure 6 Package Mechanical Layout

5.2 Packaging Information

Table 3 Packaging Information	
PACKAGE INFORMATION	
Package Acronym	PQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-029
JEDEC Option	FA-1
Maximum Lead Co-planarity	0.003 inches (0.08 mm)
Weight	5.7 g
Moisture Sensitivity Level	Printed on moisture barrier bag

5.3 Packaging Dimension Formats & Units

Table 4 Package Outline Units	
PACKAGE OUTLINE UNITS	
Unit	**Description**
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates square feature for a package with equal length and width dimensions.

5.4 Part Symbol

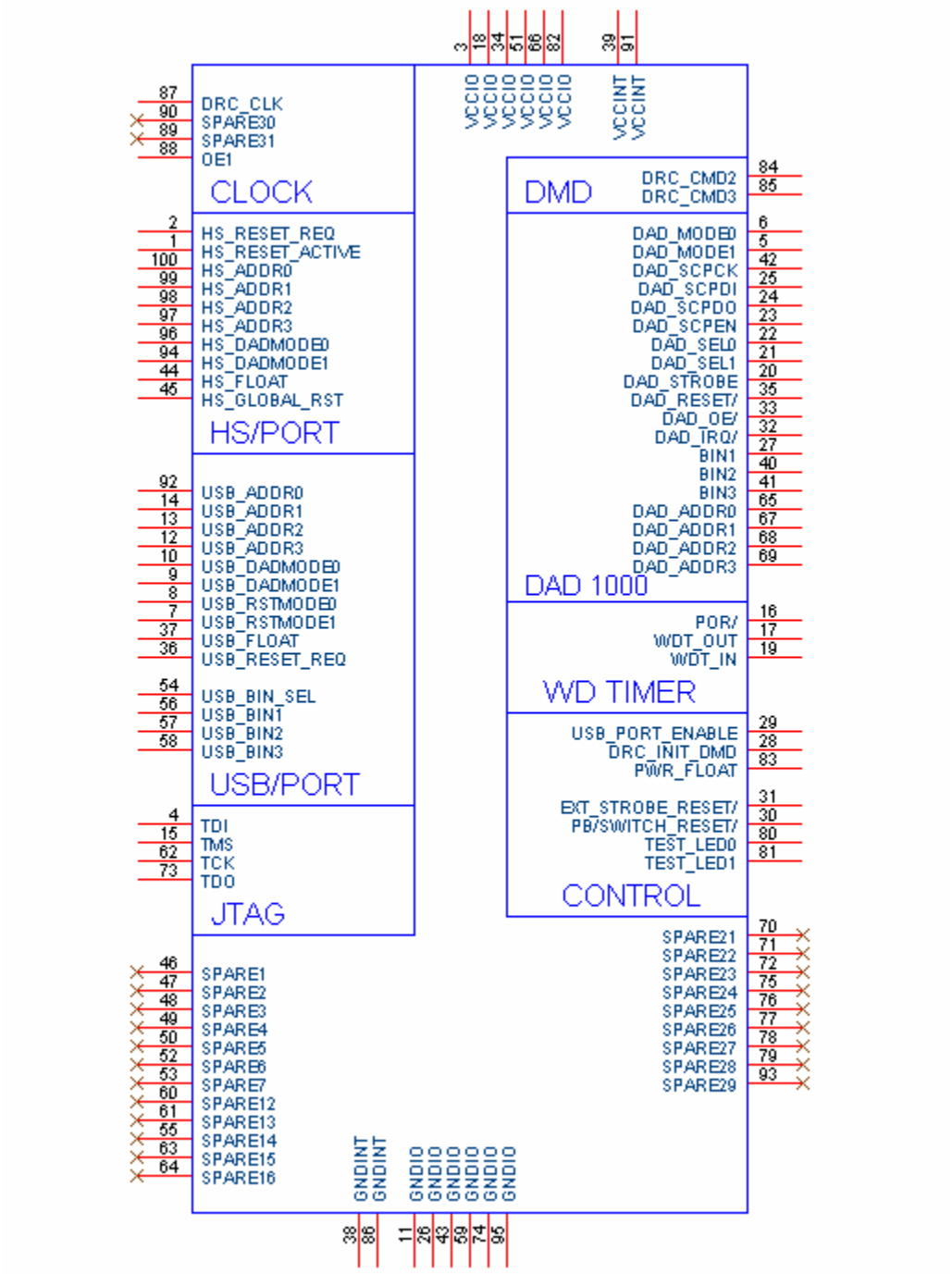


Figure 7 Part Symbol

6 General Electrical Requirements

6.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground	-0.5	3.6	V
V_{CCIO}	Supply voltage		-0.5	3.6	V
V_I	DC input voltage	*(1)*	-2.0	4.6	V
I_{OUT}	DC output current, per pin		-33	50	mA
T_{SIG}	Storage temperature	No bias	-65	150	° C
T_A	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	Under bias	-65	135	° C

6.2 Recommended Operating Conditions

Table 6 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(2)*	-0.5	3.9	V
V_O	Output voltage	Under bias	0	V_{CCIO}	V
T_A	Ambient temperature		0	55	° C
T_J	Junction temperature		0	65	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

6.3 Device DC Operating Conditions

Table 7 Device DC Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	3.9	V
V_{IL}	Low-level input voltage		-0.5	0.8	V
V_{OH}	3.3-V high-level CMOS output voltage	I_{OH} = —0.1 mA DC, V_{CCIO} = 3.00 V ***(3)***	V_{CCIO} -0.2		V
V_{OL}	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V ***(4)***		0.2	V
I_I	Input leakage current	V_I = -0.5 to 3.9 V ***(5)***	-10	10	µA
I_{OZ}	Tri-state output off-state current	V_I = -0.5 to 3.9 V ***(5)***	-10	10	µA

Notes to tables:

(1) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(2) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before VCCINT and VCCIO are powered.

(3) The parameter is measured with 50% of the outputs each sourcing the specified current. The I OH parameter refers to high-level CMOS output current.

(4) The parameter is measured with 50% of the outputs each sinking the specified current. The I OL parameter refers to low-level CMOS output current.

(5) This value is specified for normal device operation. The maximum leakage current during power-up is ±300 µA.

7 TIMING CHARACTERISTICS

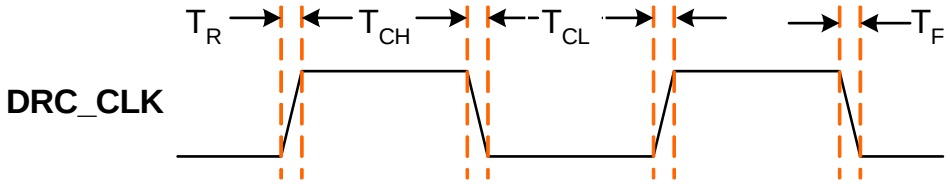


Figure 8 DRC_CLK Timing

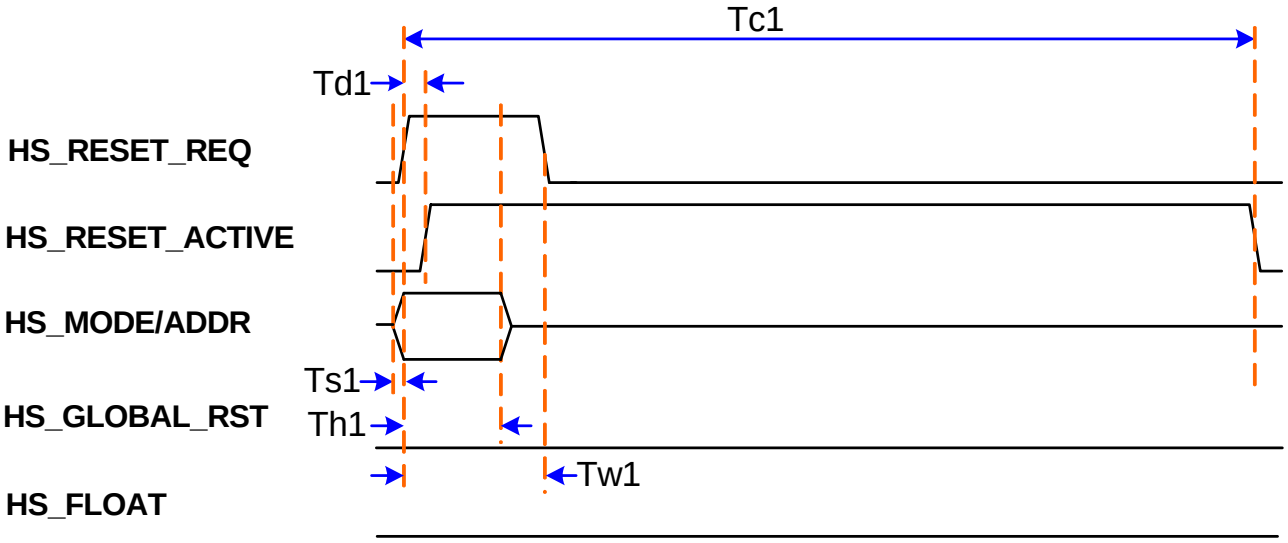


Figure 9 Reset Timing

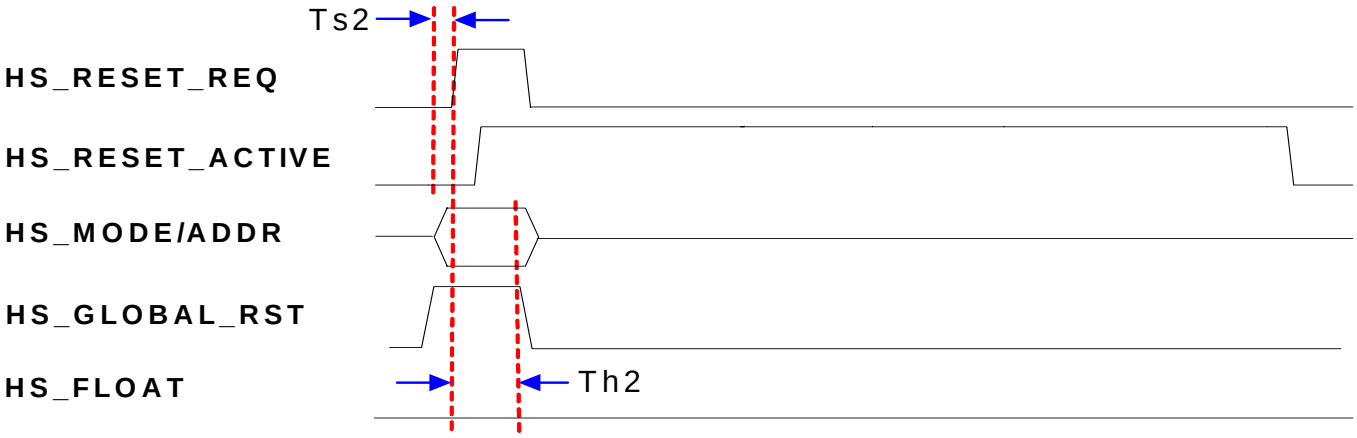


Figure 10 Global Reset Timing

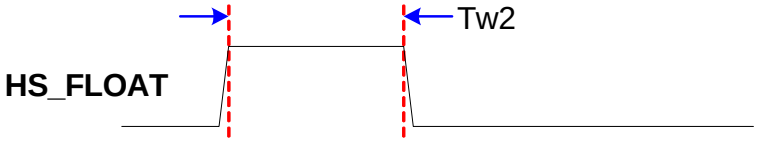


Figure 11 Float Timing

7.1 Internal Timing Characteristics

Table 8 Internal Timing Characteristics				
Parameter		**Min**	**Max**	**Unit**
TR	DRC_CLK rise time		2.0	ns
TF	DRC_CLK Fall time		2.0	ns
TCH	DRC_CLK high time	4.0		ns
TCL	DRC_CLK low time	4.0		ns
TCNT	DRC_CLK Period	16.66	16.67	ns
Tc1	HS_RESET_REQ High to HS_RESET_ACTIVE low	6.2	6.4	us
Ts1	Setup of HS_MODE and HS_ADDR before rising edge of HS_RESET_REQ	0		ns
Td1	HS_RESET_REQ to HS_RESET_ACTIVE delay	90	166	ns
Th1	Hold time : HS_MODE and HS_ADDR after rising edge of HS_RESET_REQ	200		ns
TW1	HS_RESET_REQ pulse width	250	500	ns
Ts2	HS_GLOBAL RESET to HS_RESET_REQ setup	0		ns
Th2	Hold time : HS_GLOBAL RESET after rising edge of HS_RESET_REQ	160		ns
Tw2	HS_FLOAT Pulse Width	2		us

8 DRC Pin Map

Table 9 DRC Pin Map

NAME	I/O	DESCRIPTION	CONNECT TO	PIN #
HS_RESET_ACTIVE	O	Indicates Reset is Active	USER OUTPUT	1
HS_RESET_REQ	I	Reset request from HS port	USER INPUT	2
VCCIO	P	VCC 3.3V	3.3 VOLT	3
TDI	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	4
DAD_MODE1	O	Selects DAD1000 MODE address	DAD PIN 2	5
DAD_MODE0	O	Selects DAD1000 MODE address	DAD PIN 3	6
USB_RSTMODE1	I	Selects internal, external, or pushbutton switch type of USB reset. See USBIFC CDS for explanation of USB reset modes	USBIFC PIN 142	7
USB_RSTMODE0	I	Selects internal, external, or pushbutton switch type of USB reset. See USBIFC CDS for explanation of USB reset modes,	USBIFC PIN 78	8
USB_DADMODE1	I	USB DAD Mode Select	USBIFC PIN 37	9
USB_DADMODE0	I	USB DAD Mode Select	USBIFC PIN 128	10
GNDIO	P	Ground	GROUND	11
USB_ADDR3	I	USB DAD Reset Block address select	USBIFC PIN 38	12
USB_ADDR2	I	USB DAD Reset Block address select	USBIFC PIN 39	13
USB_ADDR1	I	USB DAD Reset Block address select	USBIFC PIN 40	14
TMS	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	15
POR/	I	Power-on reset	USER INPUT	16
WDT_OUT	I	Watchdog Strobe Out	USER INPUT	17
VCCIO	P	VCC 3.3V	3.3 VOLT	18
WDT_IN	O	Watchdog Timer input	USER OUTPUT	19
DAD_STROBE	O	Latches all DAD1000 address bits and MBRST output values	DAD PIN 15	20
DAD_SEL1	O	Select DAD MBRST output voltage	DAD PIN 4	21
DAD_SEL0	O	Select DAD MBRST output voltage	DAD PIN 5	22
DAD_SCPEN	O	SCP Enable	DAD PIN 58	23
DAD_SCPDO	I	SCP data out, not used	DAD PIN 42	24
DAD_SCPDI	O	SCP Data in	DAD PIN 57	25
GNDIO	P	Ground	GROUND	26
BIN1	I	External input from to select DAD1000 voltage bin	1K Pull Up	27
INIT_DMD	O	Indicates DMD is in Initialization	HSC PIN 8	28
USB_PORT_ENABLE	I	Selects between USB and high-speed interface reset commands	USBIFC PIN 136	29
PB/SWITCH_RESET/	I	Sends reset command from pushbutton switch, must be pulled up - USB only. See USBIFC CDS for explanation of USB reset modes.	USER INPUT	30
EXT_STROBE_RESET/	I	Sends reset command from external source, must be pulled up – USB only. See USBIFC CDS for explanation of USB reset modes.	USER INPUT	31
DAD_IRQ/	I	DAD1000 interrupt request. This signal is not used	DAD PIN 43	32
DAD_OE/	O	This signal enables the DAD reset outputs	DAD PIN 6	33
VCCIO	P	VCC 3.3V	3.3 VOLT	34
DAD_RESET/	O	Resets DAD1000. Active LOW. This signal is not used. It is pulled HIGH in the controller	DAD PIN 59	35
USB_RESET_REQ	I	DAD Reset Request from USB Controller	USBIFC PIN 131	36

Table 9 DRC Pin Map				
NAME	**I/O**	**DESCRIPTION**	**CONNECT TO**	**PIN #**
USB_FLOAT	I	Float Request from USB Controller	USBIFC PIN 137	37
GNDINT	P	Ground	GROUND	38
VCCINT	P	VCC 2.5V	2.5 VOLT	39
BIN2	I	External input from to select DAD1000 voltage bin	1K Pull Up	40
BIN3	I	External input from to select DAD1000 voltage bin	1K Pull Up	41
DAD_SCPCK	O	DAD1000 Control Signal	DAD PIN 56	42
GNDIO	P	Ground	GROUND	43
HS_FLOAT	I	Float request from HS port	USER INPUT	44
HS_GLOBAL_RST	I	HS Global Reset Request	USER INPUT	45
SPARE1	-	Reserved	OPEN	46
SPARE2	-	Reserved	OPEN	47
SPARE3	-	Reserved	OPEN	48
SPARE4	-	Reserved	OPEN	49
SPARE5	-	Reserved	OPEN	50
VCCIO	P	VCC 3.3V	3.3 VOLT	51
SPARE6	-	Reserved	OPEN	52
SPARE7	-	Reserved	OPEN	53
USB_BIN_SEL	I	Reserved, must be pulled up to 3.3V.	USBIFC PIN 54	54
SPARE14	-	Reserved	OPEN	55
USB_BIN1	I	Reserved, leave open if USB not used.	USBIFC PIN 56	56
USB_BIN2	I	Reserved, leave open if USB not used.	USBIFC PIN 57	57
USB_BIN3	I	Reserved, leave open if USB not used.	USBIFC PIN 58	58
GNDIO	P	Ground	GROUND	59
SPARE12	-	Reserved	OPEN	60
SPARE13	O	Reserved	OPEN	61
TCK	I	JTAG – Pull down with 1k ohm to ground.	See Note 1	62
SPARE15	-	Reserved	OPEN	63
SPARE16	-	Reserved	OPEN	64
DAD_ADDR0	O	Selects DAD1000 BLOCK address	DAD PIN 19	65
VCCIO	P	VCC 3.3V	3.3 VOLT	66
DAD_ADDR1	O	Selects DAD1000 BLOCK address	DAD PIN 18	67
DAD_ADDR2	O	Selects DAD1000 BLOCK address	DAD PIN 17	68
DAD_ADDR3	O	Selects DAD1000 BLOCK address	DAD PIN 16	69
SPARE21	-	Reserved	OPEN	70
SPARE22	-	Reserved	OPEN	71
SPARE23	-	Reserved	OPEN	72
TDO	O	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	73
GNDIO	P	Ground	GROUND	74
SPARE24	-	Reserved	OPEN	75
SPARE25	-	Reserved	OPEN	76
SPARE26	-	Reserved	OPEN	77
SPARE27	-	Reserved	OPEN	78
SPARE28	-	Reserved	OPEN	79
TEST_LED0	O	Indicates when initialization of DMD is complete. Tracks with INIT-DMD signal	USER OUTPUT	80
TEST_LED1	O	Heartbeat to indicate state machines are running	USER OUTPUT	81

Table 9 DRC Pin Map				
NAME	**I/O**	**DESCRIPTION**	**CONNECT TO**	**PIN #**
VCCIO	P	VCC 3.3V	3.3 VOLT	82
PWR_FLOAT	I	On power-down floats mirrors on DMD	USER INPUT	83
DRC_CMD2	O	DAD1000 Control Signal	DMD PIN AC25	84
DRC_CMD3	O	DAD1000 Control Signal	DMD PIN AA25	85
GNDINT	P	Ground	GROUND	86
DRC_CLK	I	60 MHZ Clock Input	60 MHZ CLOCK	87
OE1	I	Output Enable	GROUND	88
SPARE31		Reserved	OPEN	89
SPARE30		Reserved	OPEN	90
VCCINT	P	VCC 2.5V	2.5 VOLT	91
USB_ADDR0	I	DAD Reset Block address select from USB Controller	USBIFC PIN 41	92
SPARE29		Reserved	OPEN	93
HS_DADMODE1	I	Selects DAD1000 MODE address	USER INPUT	94
GNDIO	P	Ground	GROUND	95
HS_DADMODE0	I	Selects DAD1000 MODE address	USER INPUT	96
HS_ADDR3	I	DAD Reset Block address select from HS port	USER INPUT	97
HS_ADDR2	I	DAD Reset Block address select from HS port	USER INPUT	98
HS_ADDR1	I	DAD Reset Block address select from HS port	USER INPUT	99
HS_ADDR0	I	DAD Reset Block address select from HS port	USER INPUT	100

Note 1. User may bring these signals to a connector for possible future use. The programmed contents of this device are protected from being changed or duplicated. Use of these signals to change the programmed contents of this device could damage the DRC and the DMD and void the warranty.

9 ACRONYMS

DAD 1000 DMD Power and Reset Driver

DDR Double Data Rate

SDR Single Data Rate

DMD Digital Micromirror Device

GUI Graphical User Interface

USB Universal Serial Bus

DRC DAD Reset Controller

HSC High-speed Controller

USBIFC USB Interface Controller

SCP Serial Communications Port

CDS Customer Data Sheet