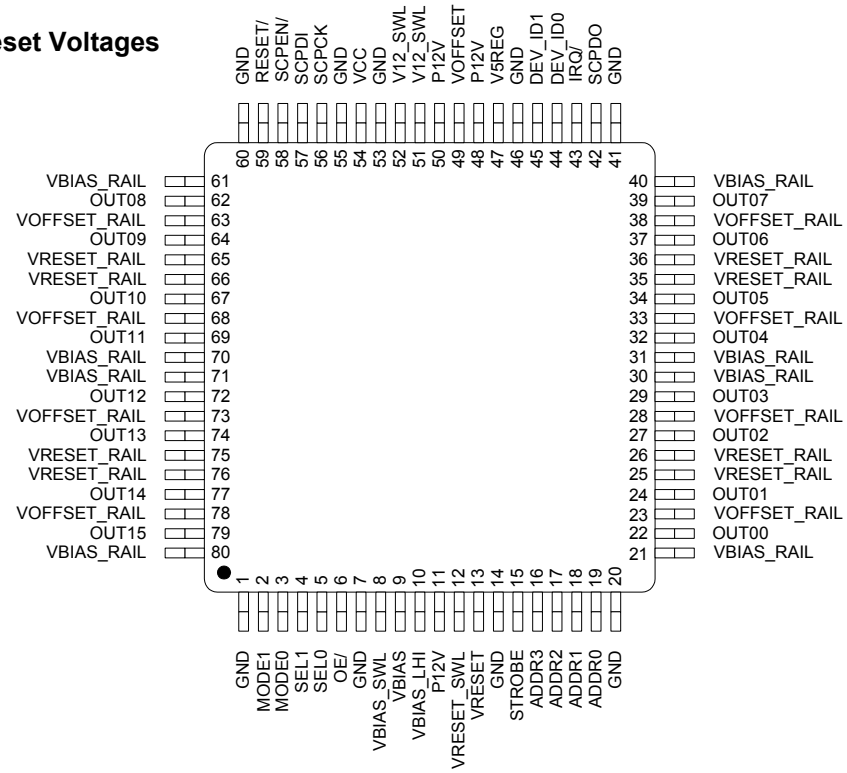
- **Provides Voltage Generation and Reset Support for DMD device**
- **Programmable Bias, Offset and Reset Voltages Increase Flexibility**
- **Optional 12V Boost Converter**
- **Thermally Enhanced Surface Mount Package**

PFP Package (top view)



Description

The DAD1000 DMD Power and Reset Driver provides the high-voltage power supplies and phased reset driver functions for a family of Digital Micro-mirror Devices (DMDs). The DAD1000 is programmable and controllable to meet all current and anticipated DMD requirements.

The high-voltage power supply function generates the three required DMD voltage levels: VBIAS, VRESET, and VOFFSET. These three supplies are programmed and controlled through a TTL and CMOS compatible serial interface. The DAD1000 also contains a +5 volt supply for internal logic functions and external color wheel control requirements.

The DAD1000 switches outputs between VBIAS, VRESET and VOFFSET voltage levels to form DMD reset waveforms. VBIAS may be supplied directly to the DMD to bias the border mirrors to the off state. VOFFSET is also supplied directly to the DMD as DMDVCC2. A fourth DMD power supply, DMDVCC, is supplied directly to the DMD by other circuitry.

The DAD1000 operates from a 12-volt power supply. If a 12-volt supply is not available, an optional boost converter function is included to generate the 12 volts from a 5-volt VCC power supply input. Adding the required external components to the circuit board enables the optional boost function.

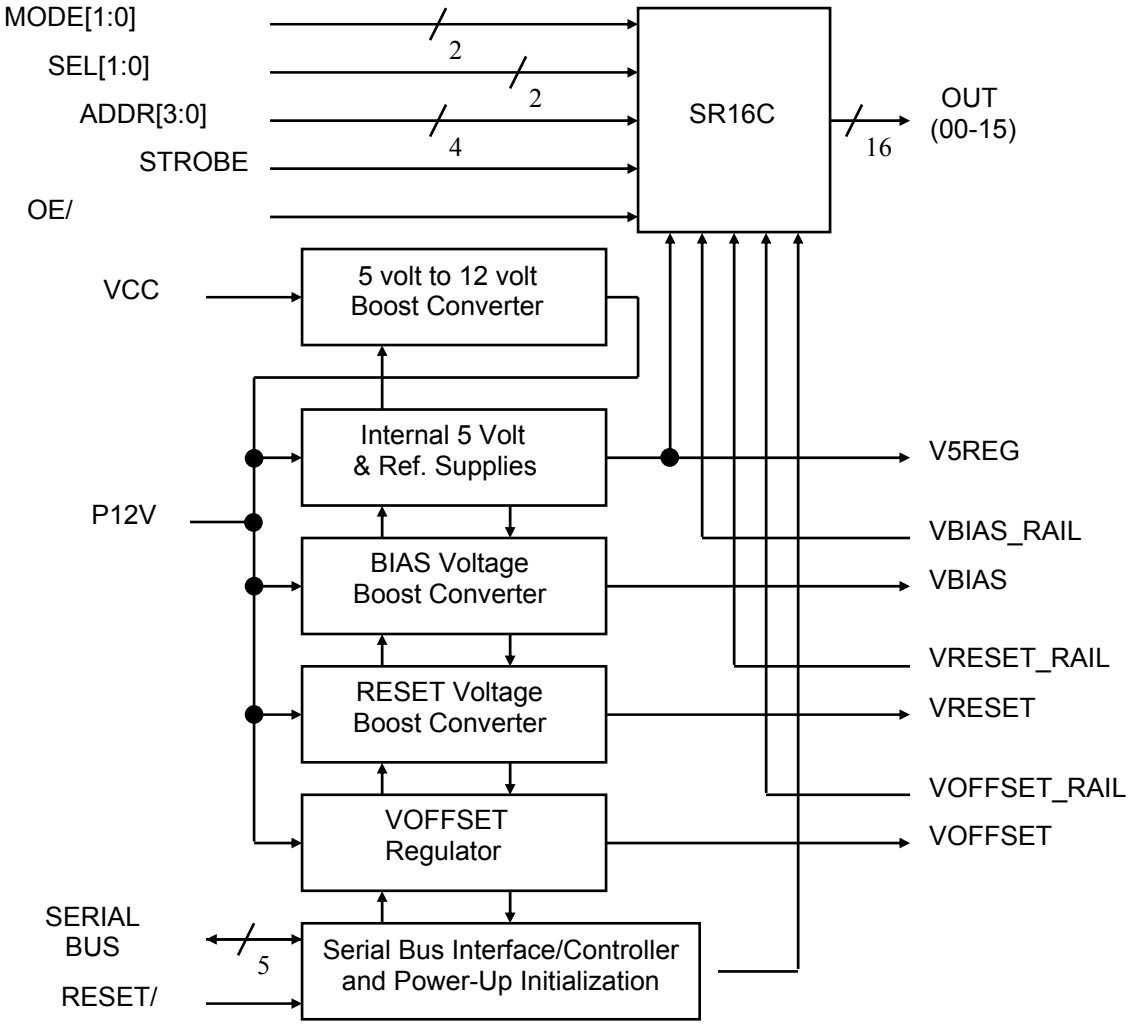
The phased reset driver function consists of a 5-volt decoder logic section controlling 16 high voltage output drivers. The logic inputs are TTL and CMOS compatible. Logic control inputs to the device are OE/, MODE(0,1), SEL(0,1), ADDR(0,3), and STROBE. The STROBE input signal latches the control information and sets up the new state on the device output pins.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

The function of the phased reset driver is to switch selected outputs between three voltage levels to generate one of several reset waveforms. The three voltage levels are the VBIAS voltage level, the VRESET voltage level, and the VOFFSET voltage level. The order of these reset waveform events is controlled externally by the logic control inputs and timed by the STROBE signal.

The DAD1000 provides a variety of reset waveform output options to the DMD using logic inputs MODE(0,1), SEL(0,1), and ADDR(0,3). The MODE(0,1) pins determine whether one, two, four, or all 16 outputs are grouped for the current operation. The ADDR(0,3) pins select the desired output group. The SEL(0,1) pins determine the output voltage level (VBIAS, VOFFSET, or VRESET). Selected outputs are tri-stated on the rising edge of the STROBE signal and latched to the selected voltage level after a break-before-make delay. Outputs will remain latched at the final voltage level until re-selected for another reset waveform cycle.

Functional block diagram



TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
ADDR0	19	I	ADDR3, ADDR2, ADDR1, and ADDR0, in conjunction with MODE[1:0], determine how the addressed and unaddressed outputs are grouped.
ADDR1	18	I	
ADDR2	17	I	
ADDR3	16	I	
VBIAS_LHI	10	I	Bias current limiter output. Switched inductor input.
VBIAS_SWL	8	I	Bias supply switch connected to bias supply switching inductor.
DEV_ID0	44	I	Serial bus device address: 00 = all; 01 = device 1; 10 = device 2; 11 = device 3.
DEV_ID1	45	I	
GND	1, 7, 14, 20, 41, 46, 53, 55, 60	O	GND is common ground. All 9 pins must all be connected to the ground plane in the PWB.
IRQ/	43	O	Interrupt request output to host processor (open drain). A 1K pull up resistor to the processor VDD supply is recommended.
MODE0	3	I	MODE0 and MODE1, in conjunction with A[3:0], determine how the addressed and unaddressed outputs are grouped.
MODE1	2	I	
OE/	6	I	Asynchronous input controls whether the 16 outputs are active or in high impedance state. OE/ = 0, Enabled. OE/ = 1, High Z. A 1K pull up to the 3.3 volt supply is desired.
OUT00	22	O	16 reset voltage waveform outputs (enabled by OE/ = 0).
OUT01	24	O	
OUT02	27	O	
OUT03	29	O	
OUT04	32	O	
OUT05	34	O	
OUT06	37	O	
OUT07	39	O	
OUT08	62	O	
OUT09	64	O	
OUT10	67	O	
OUT11	69	O	
OUT12	72	O	
OUT13	74	O	
OUT14	77	O	
OUT15	79	O	
RESET/	59	I	Asynchronous input resets DAD1000.
SCPCK	56	I	Serial bus clock. Provided by host processor.
SCPDI	57	I	Serial bus data input. Clocked in on falling edge of SCPCK.
SCPDO	42	O	Serial bus data output (open drain). Clocked out on SCPCK rising-edge. A 1K pull up resistor to the processor VDD supply is recommended.
SCPEN/	58	I	Active low enables serial bus data transfers.
SEL0	5	I	SEL1, and SEL0 determine which level of output voltage to apply to the addressed and unaddressed outputs.
SEL1	4	I	
STROBE	15	I	A rising edge latches in the control signals after a tri-state delay.
P12V	11, 48, 50	I	P12V is the main power input to DAD1000. If boost converter is used P12V is the boost supply output. All 3 pins must be connected together in the PWB.
V12_SWL	51, 52	I	Boost supply switch connected to boost supply switching inductor. Connect both pins.
V5REG	47	O	V5REG is the 5-volt logic supply output.
VBIAS_RAIL	21, 30, 31, 40, 61, 70, 71, 80	I	Bias voltage input to SR16 block. Isolated internally from VBIAS. All 8 pins must be connected together in the PWB, then connected to VBIAS.
VBIAS	9	O	VBIAS is the first of three DMD power supplies.
VCC	54	I	VCC is the boost supply input. This pin is tied to VCC when the boost supply is used to generate the 12 volts required by other supply modules. Ground this pin otherwise.
VOFFSET_RAIL	23, 28, 33, 38, 63, 68, 73, 78	I	Offset voltage input to SR16 block. Isolated internally from VOFFSET. All 8 pins to be connected together in the PWB, then connected to VOFFSET.
VOFFSET	49	O	VOFFSET is the third of three DMD voltage supplies.
VRESET_RAIL	25, 26, 35, 36, 65, 66, 75, 76	I	Reset voltage input to SR16 block. Isolated internally from VRESET. All 8 pins must be connected together in the PWB, then connected to VRESET.
VRESET	13	O	VRESET is the second of three DMD voltage supplies (tied to substrate).
VRESET_SWL	12	I	Reset supply switch connected to reset supply switching inductor.

Absolute maximum ratings over the recommended operating case temperature range (unless otherwise noted) †

Supply voltage range, VCC (see Note 1)	4.5V to 5.5 V
12V supply voltage range, P12V (see Note 1)	10.8V to 13.2 V
Logic input voltage range, V_I	-0.3 V to 7 V
Continuous total dissipation	2.8 W
Operating virtual junction temperature range, T_J	0°C to 150°C
Operating ambient temperature range, T_A	0°C to 75°C
Storage temperature range, T_{STG}	-55°C to 125°C
Lead temperature for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
NOTES: 1. All voltage values are with respect to GND.

Caution: Electrostatic Discharge Sensitive Device

The DAD1000 2503253-2 meets JEDEC standard JESD22-A114-B requirements for ESD CLASS 1B devices. The DAD1000 2503253-3 meets JEDEC standard JESD22-A114-B requirements for ESD CLASS 2 devices. Handling requirements for these devices are defined in JEDEC standard JESD625-A.

Package Specification Document

Package information and wave solder profiles for the DAD1000 is included in TI document “PowerPAD Thermally Enhanced Package: Technical Brief SLMA002”. It can be found at http://www.ti.com/sc/docs/package/related.htm or searched for at http://www.ti.com/ under the name “slma002.pdf”.

Recommended operating conditions

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage, VCC	4.75		5.25	V
Supply voltage, P12V	11.4		12.6	V
Logic low-level input current			1	µA
Logic high-level input voltage, V_{IH}	2.0			V
Low-level input voltage, V_{IL}			0.8	V
Operating ambient temperature, T_A	0		75	°C

Warning: Board layout and routing guidelines must be followed explicitly and all external components used must be in the range of values and of the quality recommended for proper operation of the DAD1000. Important: Thermal pad(s) must float or be tied to VRESET, do not connect to ground.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Electrical characteristics, VCC = 5V, T_C = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{PUC}	Power-up clear voltage	VCC = 5.5V; V_I = VCC;	no load	3.3		4.0	V
V_{OL}	Logic output low level	I_{OL} = 1mA				0.4	V
$I_{I(PU)}$	Input pull-up current	V5REG = 5V,	V_I = 5V	10		50	µA
$I_{I(PD)}$	Input pull-down current	V5REG = 5V,		10		50	µA
T_{TSD}	Thermal Shutdown Set Points	Temperature rising Temperature falling		160 145	175 160	190 175	°C
T_W	Thermal Warning Set Points	Temperature rising Temperature falling		145 130	160 145	175 160	°C

12V boost converter

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(VCC)}$	Supply current	VCC = 4.5V to 5.5V		22		750	mA
$V_{(P12V)}$	Boost converter output voltage	VCC = 4.5V to 5.5V	no load	11.4	12.0	12.6	V
$V_{(P12V\_ripple)}$	Boost converter output ripple voltage	VCC = 4.5V to 5.5V	no load			0.5	Vp-p
$I_{(P12V)}$	Boost converter output current	VCC = 4.5V to 5.5V		8		220	mA

Internal 5V regulator

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(P12V)}$	Supply current	P12V = 10.8V to 13.2V		2		50	mA
$V_{(V5REG)}$	5V regulator output voltage	P12V = 10.8V to 13.2V	no load	4.75	5.0	5.25	V
$V_{(5\_ripple)}$	5V regulator output ripple voltage	P12V = 10.8V to 13.2V	no load			0.1	Vp-p
$I_{(V5REG)}$	5V regulator output current	P12V = 10.8V to 13.2V	Internal load	1		20	mA
			External load			30	mA
$I_{(V5REG)}$	5V regulator current limit			80			mA

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Bias voltage converter

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(P12V)}$	Supply current	P12V = 10.8V to 13.2V		2		100	mA
$V_{(VBIAS)}$	Bias regulator programmable output voltage range	P12V = 10.8V to 13.2V	no load	18.5		26.5	V
$V_{(B\_ripple)}$	Bias regulator output ripple voltage	P12V = 10.8V to 13.2V	no load			0.2	Vp-p
$I_{(VBIAS)}$	Bias regulator output current	P12V = 10.8V to 13.2V	Internal load			10	mA
			external load			5	mA
$I_{(B\_LIM)}$	Bias regulator current limit			30			mA
$V_{(B\_UVSD)}$	Bias regulator under voltage shutdown			85		90	%

Reset voltage converter

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(P12V)}$	Supply current	P12V = 10.8V to 13.2V				60	mA
$V_{(VRESET)}$	Reset regulator programmable output voltage range	P12V = 10.8V to 13.2V	no load	-26.5		-18.5	V
$V_{(R\_ripple)}$	Reset regulator output ripple voltage	P12V = 10.8V to 13.2V	no load			0.2	Vp-p
$I_{(VRESET)}$	Reset regulator output current	P12V = 10.8V to 13.2V	Internal load			10	mA
$I_{(R\_LIM)}$	Reset regulator current limit			20			mA
$V_{(R\_UVSD)}$	Reset regulator under voltage shutdown			85		90	%

Offset voltage converter

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$I_{(P12V)}$	Supply current	P12V = 10.8V to 13.2V		2		40	mA
$V_{(VOFFSET)}$	Offset regulator programmable output voltage range	P12V = 10.8V to 13.2V	no load	4.25		8.25	V
$V_{(O\_ripple)}$	Offset regulator output ripple voltage	P12V = 10.8V to 13.2V	no load			0.1	Vp-p
$I_{(VOFFSET)}$	Offset regulator output current	P12V = 10.8V to 13.2V	Internal load			10	mA
			External load			30	mA
$I_{(O\_LIM)}$	Offset regulator current limit			60			mA
$V_{(O\_UVSD)}$	Offset regulator under voltage shutdown			85		90	%

Switching characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{VBIAS}, f_{VRESET}	VBIAS and VRESET switching frequency			1.5		MHz
f_{P12V}	P12V switching frequency			375		KHz

Thermal resistance

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
$R_{\theta JA}$	Junction–to–ambient thermal resistance	All outputs with equal power		27	°C/W
$R_{\theta JC}$	Junction–to–case thermal resistance	All outputs with equal power		5	°C/W

Ordering Information

T_A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING	DESCRIPTION
0°C to 70°C	PFP (S-PQFP-G80)	Tray	2503253-2	DAD1000 2503253-2	
		Tray	2503253-3	DAD1000 2503253-3	Replaces 2503253-2

Manufacturing Control Document

2503253

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

PRINCIPLES OF OPERATION

12V boost converter

The VCC to 12-volt boost converter boosts nominal 5-volt VCC levels to the 12-volt level required by other circuits in the DAD1000. This is an optional feature that may be utilized by supplying power to the VCC pin (pin 54) and adding an external inductor, a diode, and 2 capacitors. If this option is used, PWB thermal pads must be used (see PWB Layout and Routing Guidelines). If the boost converter is not used, the VCC pin should be grounded.

Figure 1 is the block diagram of this converter. See the “Component Selection Guidelines” section for recommended component values.

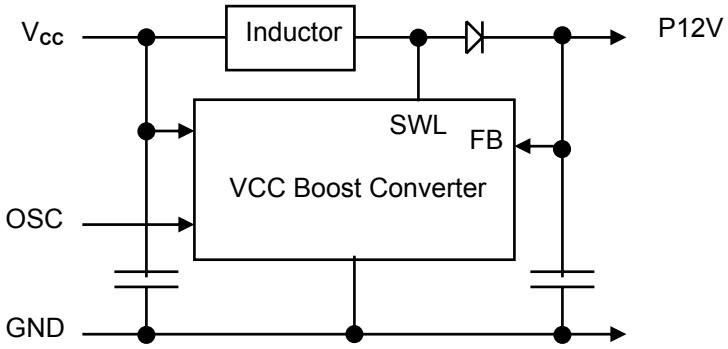


Figure 1. 12 Volt Boost Converter Block Diagram

PRINCIPLES OF OPERATION

Internal 5V regulator

The 5 volt and reference supply module contains a 5-volt linear regulator, a band gap reference supply, and a master oscillator. The linear regulator supplies the 5-volt requirement of the DAD1000 internal logic. The band gap reference supplies the reference voltage requirements for the 5-volt regulator. This reference voltage is factory trimmed to meet output voltage accuracy requirements. The master oscillator provides a clock frequency for internal logic and a reference frequency for synchronizing or driving all internal power supply switching waveforms.

Figure 2 is the block diagram of this module. See the “Component Selection Guidelines” section for recommended component values.

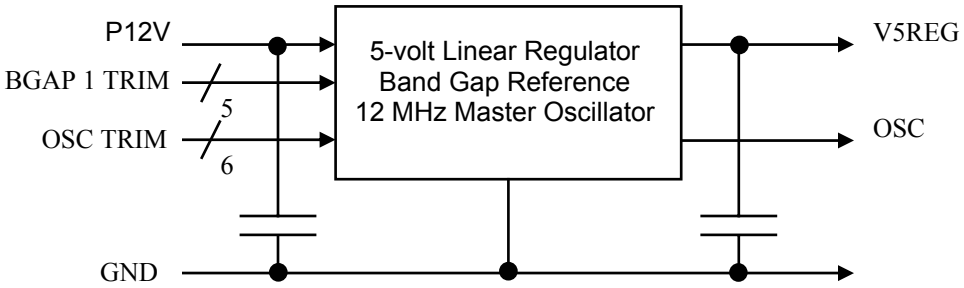


Figure 2. Internal 5 Volt Supply Block Diagram

PRINCIPLES OF OPERATION

Bias voltage boost converter

The bias voltage switching converter operates at 1/8 the master oscillator frequency. It supplies the internal bias voltage for the SR16 module and the external VBIAS for the DMD border mirrors. It is controllable and programmable through the serial interface. Three control bits select the voltage level while a fourth bit is the on/off control. The module provides 2 status bits to indicate under-voltage and current-limit conditions.

Figure 3 is the block diagram of this module. See the “Component Selection Guidelines” section for recommended component values.

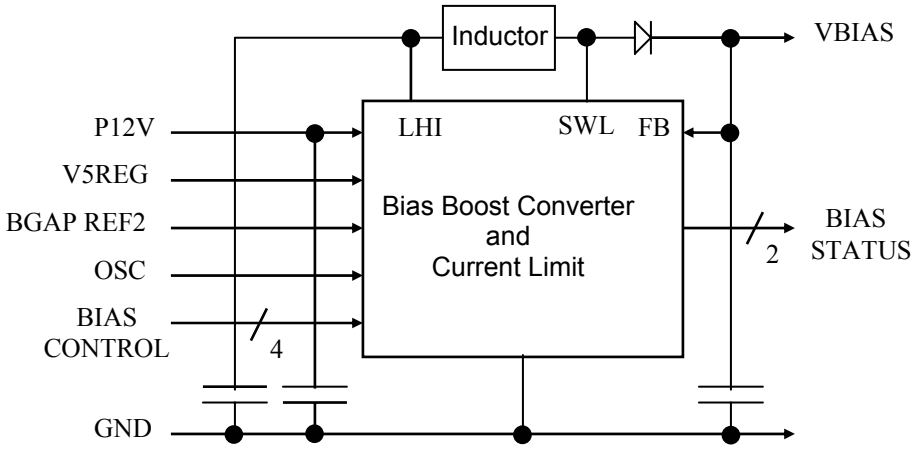


Figure 3. Bias Voltage Boost Converter Block Diagram

PRINCIPLES OF OPERATION

Reset voltage flyback boost converter

The reset voltage flyback switching converter operates at 1/8 the master oscillator frequency. It supplies the internal reset voltage levels for the SR16 module. It is controllable and programmable through the serial interface. Three control bits select the voltage level while a fourth bit is the on/off control. The module provides 2 status bits to indicate under-voltage and current-limit conditions.

Figure 4 is the block diagram of this module. See the "Component Selection Guidelines" section for recommended component values.

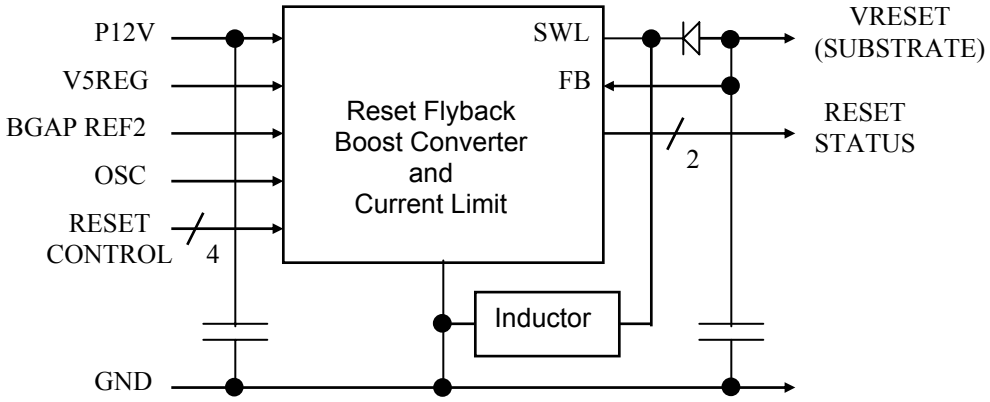


Figure 4. Reset Voltage Flyback Boost Converter Block Diagram

PRINCIPLES OF OPERATION

Offset voltage regulator

The VOFFSET/DMDVCC2 module is a linear regulator. It supplies the internal VOFFSET voltage for the SR16 module and the external DMDVCC2 for the DMD. It is controllable and programmable through the serial interface. Four control bits select the voltage level while a fifth bit is the on/off control. The module provides 2 status bits to indicate under-voltage and current-limit conditions.

Figure 5 is the block diagram of this module. See the "Component Selection Guidelines" section for recommended component values.

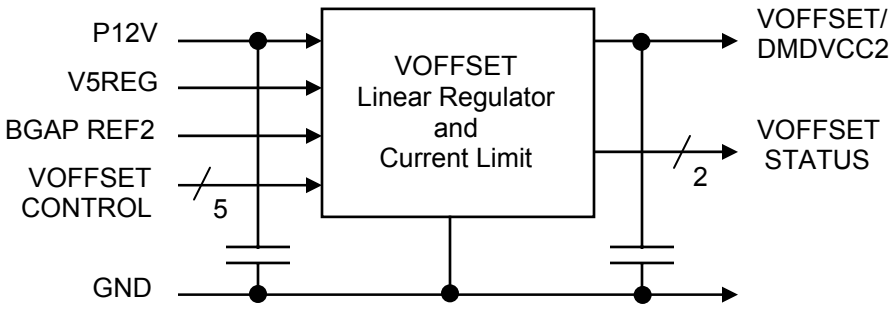


Figure 5. Bias Voltage Boost Converter Block Diagram

PRINCIPLES OF OPERATION

Serial Communications Port (SCP)

The Serial Communications Port (SCP) is a full duplex, synchronous, character-oriented (byte) port that allows exchange of data between the master ASIC and one or more slave DAD1000s (and/or other DLP™ devices).

Table 1. Serial Communications Port Signal Definitions.

Signal	I/O	From/To	Type	Description
SCPCK	I	SCP bus master to slave.	LVTTL compatible	SCP bus serial transfer clock. The host processor (master) generates this clock.
SCPEN/	I	SCP bus master to slave.	LVTTL compatible	SCP bus access enable (low true). When high, slave will reset to idle state, and SCPDO output will tri-state. Pulling SCPEN/ low initiates a read or write access. SCPEN/ must remain low for an entire read/write access, and must be pulled high after the last data cycle. To abort a read or write cycle, pull SCPEN/ high at any point.
SCPDI	I	SCP bus master to slave.	LVTTL compatible	SCP bus serial data input. Data bits are valid and must be clocked in on the falling edge of SCPCK.
SCPDO	O	SCP bus slave to master	LVTTL, open drain w/tri-state	SCP bus serial data output. Data bits must clocked out on the rising edge of SCPCK. A 1K pull up resistor to the 3.3-volt ASIC supply is required.
IRQ/	O	SCP bus slave to master	LVTTL, open drain	Not part of the SCP bus definition. Asynchronous interrupt signal from slave to request service from master. A 1K pull up resistor to the 3.3-volt ASIC supply is required.

Table 2. Serial InterfaceTiming.

Description	Minimum	Nominal	Maximum
Slave enable to control byte	360 ns		
Byte to byte (nominally 1 SCPCK cycle)	1.9 usec		
Last byte to slave disable	360 ns		
SCPCK period (nominal frequency is 500 KHz)	1.9 usec	2 usec	2.1 usec
SCPCK high or low time	0.3 usec		
SCPDI set-up and hold time (ref falling edge of SCPCK)	-0.3 usec		0.3 usec
SCPDO propagation delay (ref rising edge of SCPCK)	0		0.3 usec

PRINCIPLES OF OPERATION

SR16C Block

The SR16 block diagram is shown in Figure 6. The SR16 block contains three banks of high-voltage switches that connect each of the 16 output pins to one of three voltage rails. Address and control decode logic determine the next output state with break-before-make operation when the strobe signal occurs. The SR16 block produces the reset waveforms required for DMD operation.

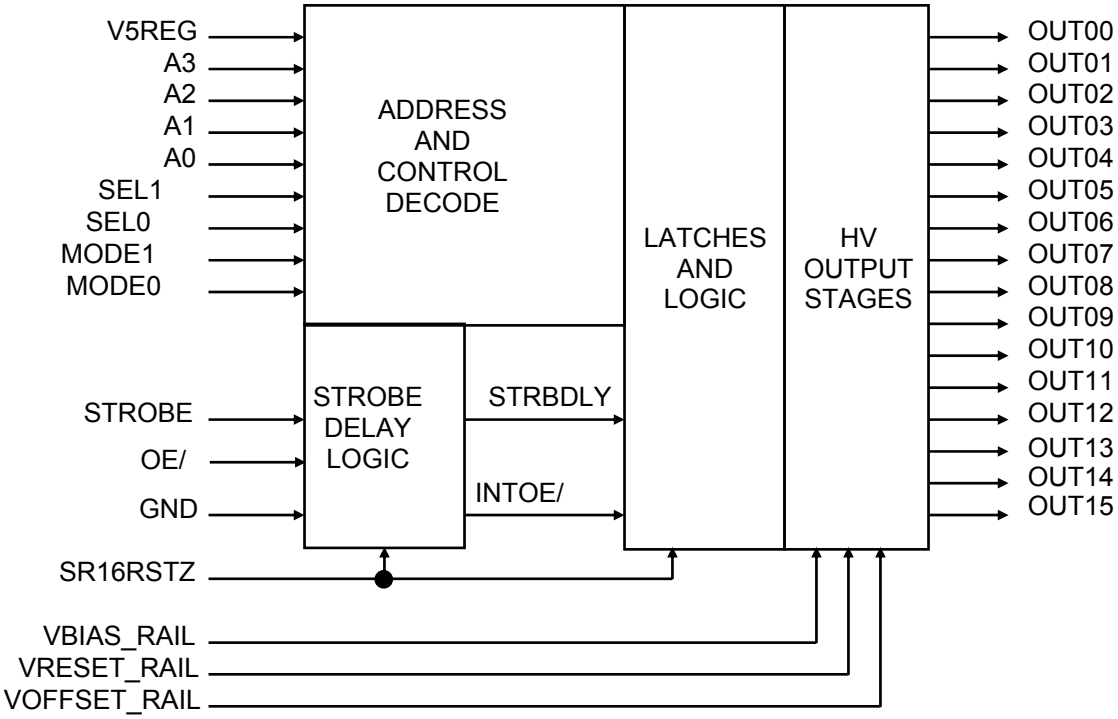


Figure 6. SR16 Phased Reset Driver Block Diagram.

PRINCIPLES OF OPERATION

Table 3. SR16 Output Stage Drive Requirements

Description	Minimum	Nominal	Maximum
Phased reset repetition frequency each pin (non-overlapping)			20 KHz
Global reset repetition frequency all pins			14.3 KHz
Output device breakdown voltage - VBIAS and VRESET level devices	60 volts		
Output device breakdown voltage – VOFFSET level devices	55 volts		
Output leakage to any rail in tri-state mode	1μA		

Table 4. SR16 Block Control Signal Timing Requirements.

Parameter	Min	Typical	Max	Unit
STROBE Pulsewidth	35			ns
Output time to high Z from OE/ pin high			100	ns
Output enable time from OE/ pin low			100	ns
A[3:0], MODE[1:0], and SEL[1:0] set-up time to STROBE edge	20			ns
A[3:0], MODE[1:0], and SEL[1:0] hold time from STROBE edge	20			ns
Propagation time - STROBE to VBIAS/VRESET edge 50% point Global mode			200 500	ns ns
Propagation time - STROBE to VRESET/VOFFSET edge 50% point Global mode			200 500	ns ns
Propagation time - STROBE to VOFFSET/VBIAS edge 50% point Global mode			200 500	ns ns

PWB LAYOUT AND ROUTING GUIDELINES

Grounding guidelines:

The PWB should have an internal ground plane that extends under the DAD1000. All 9 ground pins (1, 7, 14, 20, 41, 46, 53, 55, and 60) must be connected to the ground plane using the shortest possible runs and vias. If the optional 12-volt boost supply is being used, etch runs and vias for pins 53 and 55 must be sized for a total current flow of 0.75 amps. All filter and bypass capacitors must be placed near the pin being filtered or bypassed for the shortest possible runs to the part and to the ground plane.

Thermal guidelines:

The DAD1000 package should be thermally bonded or soldered to an external thermal pad on the PWB surface. The recommended dimensions of the thermal pad are 10 x 10 mm centered under the part. The metal bottom of the package is tied internally to the substrate at the VRESET voltage level. **Therefore, the thermal pad on the board must be isolated from any other circuit or ground and no circuit vias are allowed inside the pad area.** The internal ground plane and any other internal VCC or VDD planes should extend under the DAD1000 to help carry the heat away. If the optional 12-volt boost converter is used, thermal pads are required on both sides of the PWB with 16 thermal vias between them. Thermal pads and the thermal vias must be isolated from ground, connected to VRESET or isolated from any other circuit.

Power supply rail guidelines:

The optional 12-volt boost converter requires up to 0.75 amps. Etch runs from the 5-volt power source to the switching inductor and VCC pin 54 and etch runs from the switching inductor to V12_SWL pins 51 and 52 must be sized accordingly. VCC filter and bypass capacitors should be placed near pin 54. Note that if this converter is not used, VCC pin 54 should be grounded.

The etch runs connecting P12V pins 11, 48, and 50 to the 12-volt power source could carry up to 0.25 amps and should be sized accordingly. P12V filter and bypass capacitors should be placed near and connected to pin 11 to be near the VBIAS and VRESET switching converters. V5REG filter and bypass capacitors must be placed near and connected to pin 47.

VBIAS_RAIL etch runs should be routed in the following order: pin 40, pin 31, pin 30, pin 21, pin 80, pin 71, pin 70, and pin 61. The etch runs should be short and direct as they must carry 50 ns current spikes of up to 0.6 amps peak. Bypass capacitors should be located near and connected to pins 30 and 71 to provide bypassing on both sides. VBIAS_LHI filter and bypass capacitors must be placed near and connected to pin 10. VBIAS filter and bypass capacitors must be placed near and connected to pin 9. VBIAS pin 9 must also be connected (optionally with a 0-ohm resistor) to VBIAS_RAIL at or between pins 21 and 80.

VRESET_RAIL etch runs should be routed in the following order: pin 36, pin 35, pin 26, pin 25, pin 76, pin 75, pin 66, and pin 65. The etch runs should be short and direct as they must carry 50 ns current spikes of up to 0.6 amps peak. Bypass capacitors should be placed near and connected to pins 35 and 66 to provide bypassing on both sides. VRESET filter and bypass capacitors must be located near and connected to pin 13. VRESET pin 13 must also be connected (optionally with a 0-ohm resistor) to VRESET_RAIL at or between pins 25 and 76.

VOFFSET_RAIL etch runs should be routed in the following order: pin 23, pin 28, pin 33, pin 38, pin 63, pin 68, pin 73, and pin 78. The etch runs should be short and direct as they must carry 50 ns current spikes of up to 0.6 amps peak. Bypass capacitors should be placed near and connected to pins 28 and 73 to provide bypassing on both sides. VOFFSET filter and bypass capacitors must be placed near and connected to pin 49. VOFFSET pin 49 must also be connected (optionally with a 0-ohm resistor) to VOFFSET_RAIL at or between pins 38 and 63.

COMPONENT SELECTION GUIDELINES

12-volt boost converter: (Applications using the optional 12-volt boost converter will need to add the following:)

Component	Value	Type or part number	Connection 1	Connection 2
Input filter capacitor	33 μF, 16 VDC; 1Ω max ESR	Tantalum or ceramic	Pos: VCC, pin 54 (locate near pin 54)	Neg: Ground plane
Input bypass capacitor	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VCC, pin 54 (locate near pin 54)	Ground plane
Inductor	6.8 μH, 2.2 amp; 75 mΩ	Coil Craft DT3316P-682 (or equivalent)	VCC, pin 54	V12_SWL, pins 51 and 52
Schottky diode	2.1 amp, 60 volt	International Rectifier 10MQ060N (or equivalent)	Anode: V12_SWL, pins 51 and 52	Cathode: P12V, pins 11, 48, and 50

5-volt regulator:

Component	Value	Type or part number	Connection 1	Connection 2
P12V filter capacitor	10 to 33 μF, 20 VDC; 1Ω max ESR	Tantalum or ceramic	Pos: P12V, pin 11 (locate near pin 11)	Neg: Ground plane
P12V bypass capacitor	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	P12V, pin 11 (locate near pin 11)	Ground plane
V5REG filter capacitor	0.1 to 1.0 μF, 10 VDC; 2.5Ω max ESR	Tantalum or ceramic	Pos: V5REG, pin 47 (locate near pin 47)	Neg: Ground plane
V5REG bypass capacitor	0.1 μF, 16 VDC; 0.1Ω max ESR	Ceramic	V5REG, pin 47 (locate near pin 47)	Ground plane

Bias voltage boost converter:

Component	Value	Type or part number	Connection 1	Connection 2
LHI filter capacitor	10 μF, 20 VDC; 1Ω max ESR	Tantalum or ceramic	Pos: VBIAS_LHI, pin 10 (locate near pin 10)	Neg: Ground plane
LHI bypass capacitor	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VBIAS_LHI, pin 10 (locate near pin 10)	Ground plane
VBIAS filter capacitor	1 to 10 μF, 35 VDC; 1Ω max ESR; (3.3 μF nominal value)	Tantalum or ceramic	Pos: VBIAS, pin 9 (locate near pin 9)	Neg: Ground plane
VBIAS bypass capacitor	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VBIAS, pin 9 (locate near pin 9)	Ground plane
VBIAS_RAIL bypass capacitors (2 required)	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VBIAS_RAIL, pins 30 and 71 (locate near pins 30 and 71)	Ground plane
Resistor jumper (optional)	0 Ω normal (1 Ω for design verification testing)	(Allows VBIAS current measurement)	VBIAS, pin 9	VBIAS_RAIL, pins 21 or 80
Inductor	22 μH, 0.5 amp; 160 mΩ	Coil Craft DT1608C-223 (or equivalent)	VBIAS_LHI, pin 10	VBIAS_SWL, pin 8
Schottky diode	0.5 amp, 40 volts (minimum)	Motorola MBR0540T1 or STMicroelectronics STPS0540Z, STPS0560Z (or equivalent)	Anode: VBIAS_SWL, pin 8	Cathode: VBIAS, pin 9

COMPONENT SELECTION GUIDELINES

Reset voltage boost converter:

Component	Value	Type or part number	Connection 1	Connection 2
VRESET filter capacitor	1 to 10 μF, 35 VDC; 1Ω max ESR; (3.3 μF nominal value)	Tantalum or ceramic	Neg: VRESET, pin 13 (locate near pin 13)	Pos: Ground plane
VRESET bypass capacitor	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VRESET, pin 13 (locate near pin 13)	Ground plane
VRESET_RAIL bypass capacitors (2 required)	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VRESET_RAIL, pins 35 and 66 (locate near pins 35 and 66)	Ground plane
Resistor jumper (optional)	0 Ω normal (1 Ω for design verification testing)	(Allows VRESET current measurement)	VRESET, pin 13	VRESET_RAIL, pins 25 or 76
Inductor	22 μH, 0.5 amp; 160 mΩ	Coil Craft DT1608C-223 (or equivalent)	VRESET_SWL, pin 12	Ground plane
Schottky diode	0.5 amp (minimum), 60 volts	STMicroelectronics STPS0560Z or International Rectifier 10MQ060N (or equivalent)	Cathode: VRESET_SWL, pin 12	Anode: VRESET, pin 13

OFFSET voltage regulator:

Component	Value	Type or part number	Connection 1	Connection 2
VOFFSET/VCC2 filter capacitors (2 required)	1 to 4.7 μF, 35 VDC; 1Ω max ESR; (3.3 μF nominal value) (different values OK but keep the sum to 6.8 μF maximum)	Tantalum or ceramic	Pos: VOFFSET, pin 49 (1st near pin 49); Pos: DMDVCC2 pins (locate 2nd at DMD)	Neg: Ground plane; Neg: Ground plane
VOFFSET/VCC2 bypass capacitors (5 required)	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VOFFSET, pin 49 (locate 1 near pin 49); DMDVCC2 pins (locate 4 at DMD)	Ground plane; Ground plane
VOFFSET_RAIL bypass capacitor (2 required)	0.1 μF, 50 VDC; 0.1Ω max ESR	Ceramic	VOFFSET_RAIL, pins 28 and 73 (locate near pins 28 and 73)	Ground plane
Resistor jumper (optional)	0 Ω normal (1 Ω for design verification testing)	(Allows VOFFSET current measurement)	VOFFSET, pin 49	VOFFSET_RAIL, pins 38 or 63
Resistor jumper (optional)	0 Ω normal (1 Ω for design verification testing)	(Allows VCC2 current measurement)	VOFFSET, pin 49	DMDVCC2 pins

Pull up resistors:

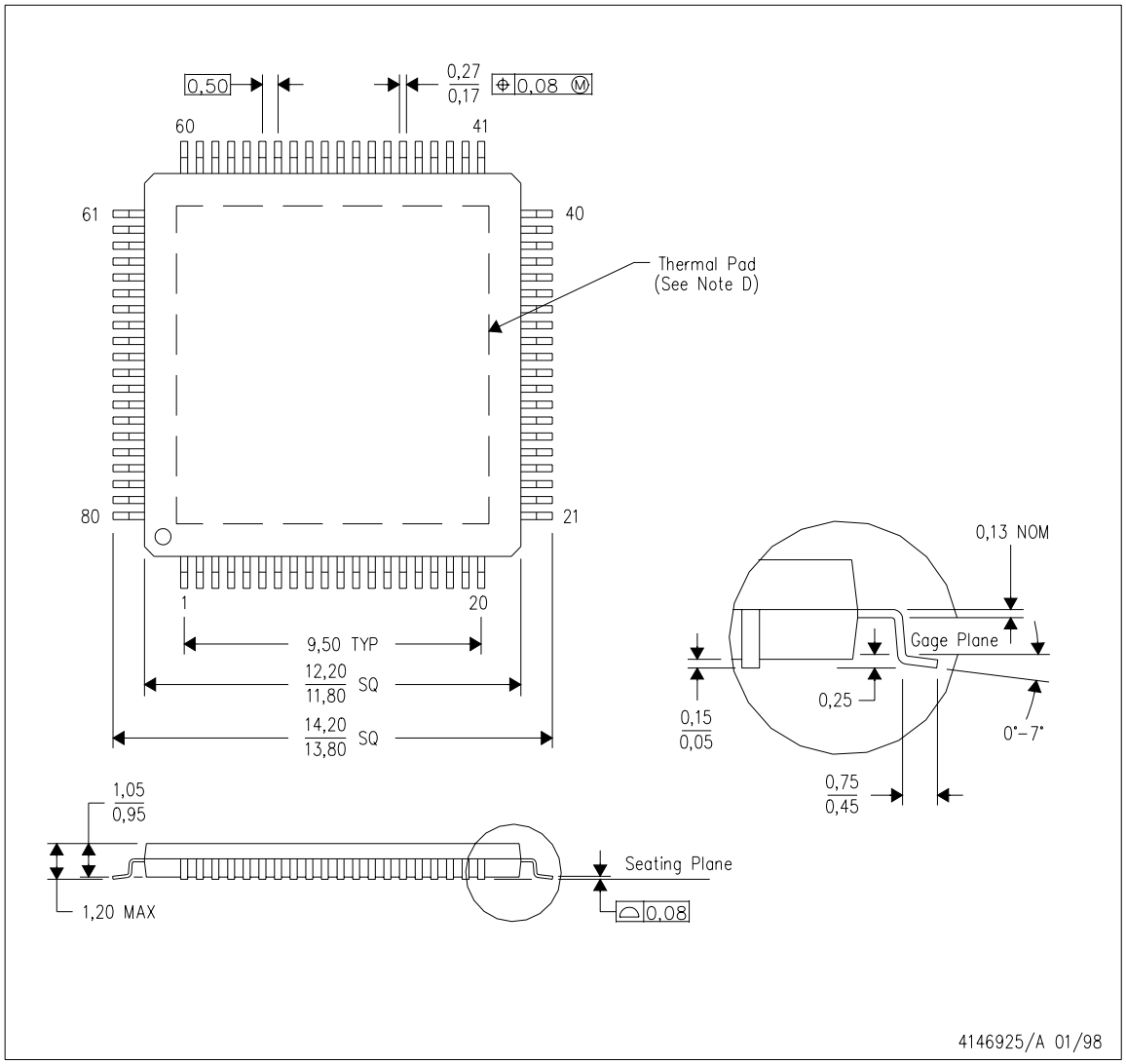
Component	Value	Type or part number	Connection 1	Connection 2
Resistor	1 KΩ		SCPDO, pin 42	3.3 volt VDD (ASIC)
Resistor	1 KΩ		IRQ/, pin 43	3.3 volt VDD (ASIC)
Resistor (optional)	1 KΩ		OE/, pin 6	3.3 volt VDD (ASIC)

Notes:

Aluminum electrolytic capacitors may not be suitable for the DAD1000 application. At the switching frequencies up to 1.5MHz used in the DAD1000, aluminum electrolytic capacitors drop significantly in capacitance and increase in ESR resulting in voltage spikes on the power supply rails. This action may cause the device to shut down or perform in an unreliable manner.

MECHANICAL DATA

PFP (S–PQFP–G80) PowerPAD™ PLASTIC QUAD FLATPACK



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. The package thermal performance may be enhanced by bonding the thermal pad to an external thermal plane. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
E. Falls within JEDEC MS–026

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

TI warrants performance of its products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Customers are responsible for their applications using TI components.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, license, warranty or endorsement thereof.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations and notices. Representation or reproduction of this information with alteration voids all warranties provided for an associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Resale of TI's products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service, is an unfair and deceptive business practice, and TI is not responsible nor liable for any such use.

Also see: Standard Terms and Conditions of Sale for Semiconductor Products. www.ti.com/sc/docs/stdterms.htm

Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265

Copyright © 2001, 2002 Texas Instruments Incorporated