Data Sheet
TI DN 2506019 REV B
October 2004

DMD Discovery™ 1100 HSC (High-Speed Controller)

This data sheet covers the functionality of the Discovery 1100 HSC (High-Speed Controller). The Discovery 1100 HSC provides the high-speed interface to the TI 0.7XGA 12° DDR DMD. The HSC provides conversion from SDR to DDR along with synchronization and high-speed control of the DMD. The controller also provides for selection between a high-speed interface and a USB interface.

Revisions		
Rev	Descriptions	Date
717-0040-001 A	Initial release	10/15/03
717-0040-001 B	Complete rewrite with more detailed design information	10/23/04
717-0040-001 C	Corrected timing and mechanical information	2/16/04
717-0040-001 D	Corrected typographical error	2/29/04
TI 2506019 A	Changed to TI drawing number system Added Note 2 toTable 11	8/13/04
TI 2506019 B	Changed LCB timing in table 10	10/4/04

IMPORTANT NOTICE

Texas Instruments and its subsidiaries (TI) reserve the right to make changes to their products or to discontinue any product or service without notice, and advise customers to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability.

In no event shall TI be liable for any special, incidental, consequential or indirect damages however caused, arising in anyway from the sale or use of the TI products. Products purchased from a TI authorized distributor are subject to the distributor's terms and conditions of sale.

TI warrants performance of its semiconductor products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements. Customers are responsible for their applications using TI components unless otherwise stated, this documentation and its intellectual content is copyrighted or provided under license and may not be distributed in any form without the express written permission of Texas Instruments Incorporated.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("critical applications"). TI semiconductor products are not designed, authorized, or warranted to be suitable for use in life-support devices or systems or other critical applications. Inclusion of TI products in such applications is understood to be fully at the customer's risk.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance or customer product design. TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used. TI's publication of information regarding any third party's products or services does not constitute TI's approval, warranty or endorsement thereof.

Trademarks

Microsoft, Windows, Microsoft ActiveX, Windows XP and Windows 2000 are trademarks of Microsoft Corporation.

Other trademarks are the property of their respective owners.

TABLE OF CONTENTS

List of Tables

List of Illustrations

1 Overview

This document covers the functionality of the Discovery 1100 HSC (High-Speed Controller). The Discovery 1100 HSC provides the high-speed interface to the TI 0.7XGA 12° DDR DMD. The HSC provides conversion from SDR to DDR along with synchronization and high-speed control of the DMD. The controller also provides for selection between a high-speed interface and a USB interface.

Shown below are two simplified block diagrams (Figure 1, Figure 2) showing the use of the Discovery 1100 HSC with and without the USB Controller and USBIFC.

The block diagram in Figure 1 is a typical system using both high-speed (HS) and USB interfaces. The DMD may be controlled from either the USB or HS interface. Buffers should be used in systems that have both USB and high-speed interfaces to separate the data busses to the DMD. The DRC provides initialization and reset logic required for the DAD1000 to drive the DMD mirror reset inputs.

The six components shown are:

DMD 0.7XGA 12° DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver for DMD
Cypress FX2 – 2.0 USB controller
Discovery 1100 USBIFC (USB Interface Controller) – provides interface between USB and DMD Components
Discovery 1100 DRC (DAD Reset Controller) – provides reset interface to DAD and DMD
Discovery 1100 HSC (High-Speed Controller) – provides high-speed clock control and command interfaces

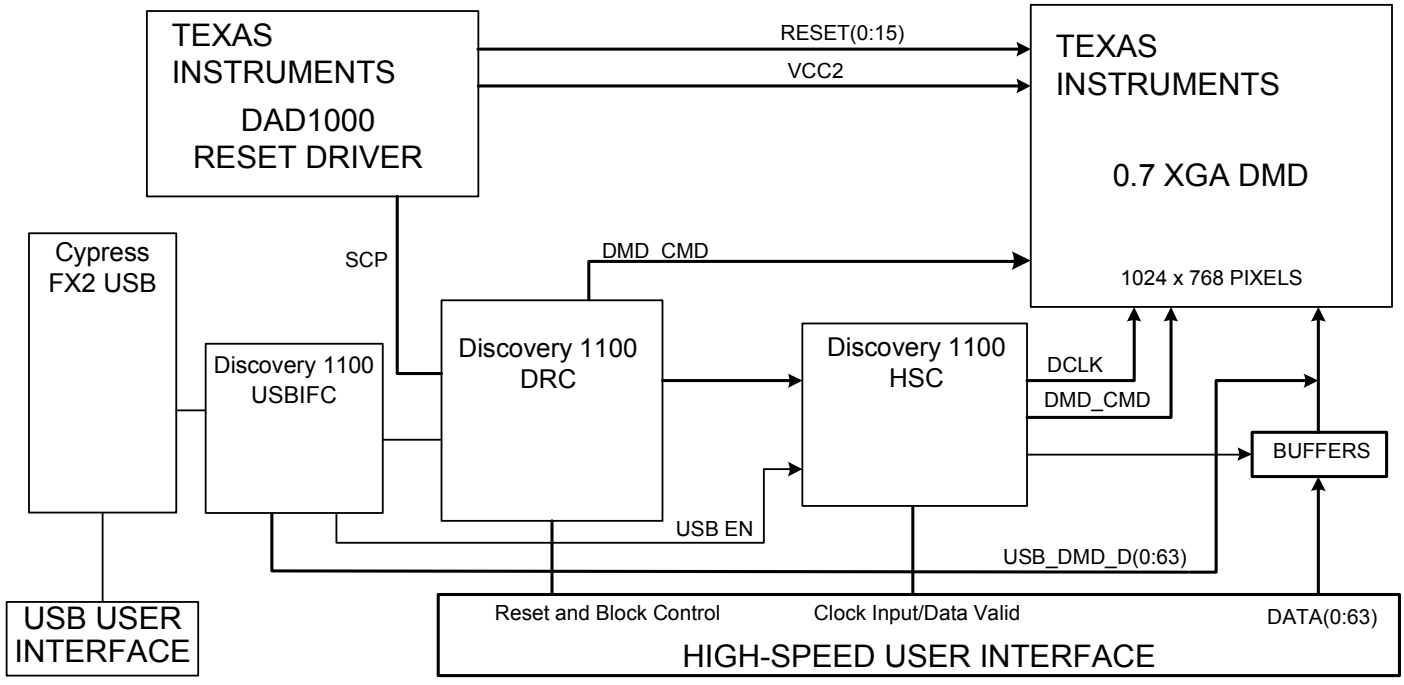


Figure 1 Discovery Block Diagram with USB

The second block diagram (Figure 2) shows a typical system using only the high-speed interface. Buffers for high-speed data are not required, but recommended if data is driven from an off board source.

The four components shown are:

DMD 0.7XGA 12° DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver for DMD
Discovery 1100 DRC (DAD Reset Controller) – provides reset interface to DAD and DMD
Discovery 1100 HSC (High-Speed Controller) – provides high-speed clock control and command interface

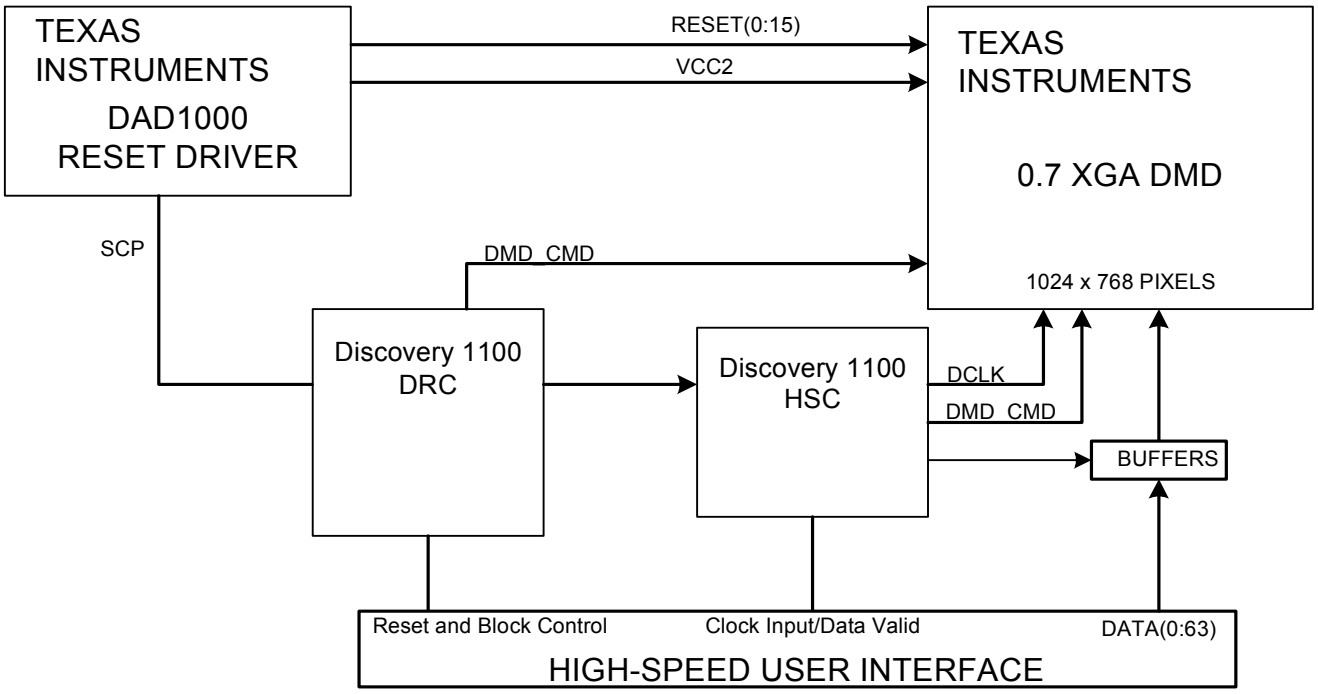


Figure 2 Discovery Block Diagram without USB

2 Functional Description

The Discovery 1100 HSC provides all of the logic necessary to control the DMD from both the HSP (High-Speed Port) and the USB components. A functional description of all signals referenced here can be found in section 3 and a functional timing diagram of data transfer and signal relations can be found in Figure 4 of section 3.

The I/O from the Discovery 1100 DMD HS Controller is divided into the following functional sections:

2.1 Clocking

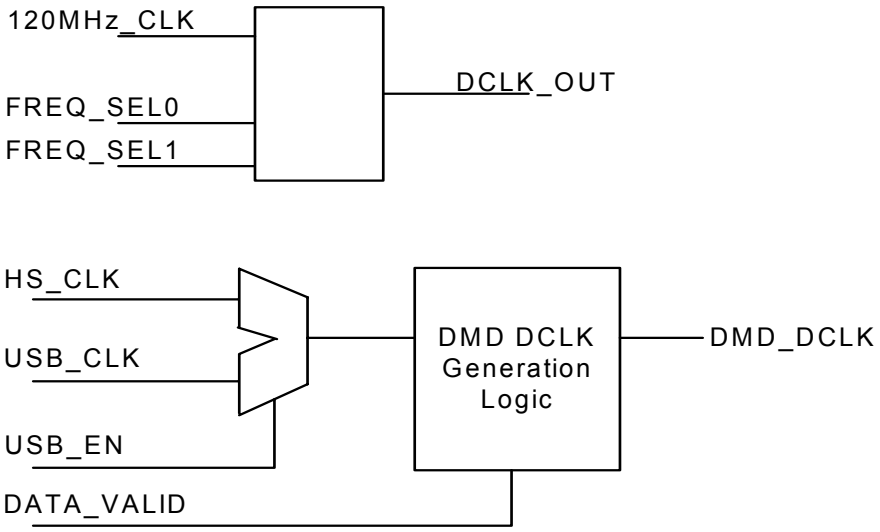


Figure 3 High-Speed Clocking Functions

The Discovery 1100 HSC has two separate clock circuits for two distinct functions. The first is a clock divider circuit that has an input labeled 120MHz_CLK. The input frequency can be any frequency up to 120MHz and can be divided by 1,2,4 or 8 and set by FREQ_SEL [0:1] to the output named DCLK_OUT. The DCLK_OUT can used to drive the HS_CLK input.

The second circuit selects from the input clock sources and combined with control signals creates the clock that drives the DMD (DMD_DCLK). In the high-speed mode (USB_EN pulled high) the input to the Discovery 1100 HSC is a SDR clock called HS_CLK. This clock can be up to 120 MHZ and is converted to DDR format with output named DMD_DCLK. This clock (DMD_DCLK) is controlled by DATA_VALID and always starts DMD_DCLK with a rising edge. This connects directly to the DMD. The timely relation between HS_CLK and DMD_DCLK is defined in Figure 8 in this document. When the USB is driving the DMD (USB_EN pulled low) the SDR clock (USB_CLK) comes from the USBIFC.

Data is transferred to the DMD using DMD_DCLK in combination with DATA_VALID and other control bits as described in sections 2 and 3.

2.2 Line and DMD Control and Miscellaneous Input and Control

The Line and DMD control functions provided by the HSC are listed below:

Line control Inputs: WRITE_EN, GLBCLRMEM, A_MODE [0:1]

These signals provide control for each line and are described in further detail in section 3.

USB control inputs: USB_DMD_CMD [0:1]

These are signals that provide functions from the USBIFC equivalent to the functions that are provided by the HSC to drive the DMD from the HS interface.

DMD control outputs: DMD_CMD0/1

These are DMD control signals that are initiated from either the HSC or USB.

The miscellaneous input and control signals are:

DRC_INIT_DMD, READYTO ACCEPT, H/SPEEDBUF_EN, LINE_SYNC, OE1

3 Electrical Interface

The following section describes the electrical interface to the Discovery 1100 HSC.

3.1 Pin Definitions

Table 1 gives a list of user available controls and status pin names and their corresponding signal names, along with a brief description of their function.

Table 1 I/O Pin Descriptions

Pin Name	Description	I/O
HS_CLK	Input clock for HS mode operation	I
DATA_VALID/	Indicates the data sent to the DMD is valid, used to start write sequence	I
WRITE_EN	Indicates the data is valid to write into DMD memory	I
GLBCLRMEM	Used to clear DMD memory 16 lines at a time.	I
A_MODE [0:1]	DMD row address counter control	I
TRC_IN	Used to invert data at DMD on a data word basis (each 64 bit data word)	I
DRC_INIT_DMD	Indicates that the DRC is in initialization, goes high when initialization is complete.	I
DRC_RESET_ACTIVE	For possible future use – output from DRC, high during DMD reset	I
READYTOACCEPT	Indicates the high-speed port is enabled and ready to accept data.	O
H/SPEEDBUF_EN/	Used to enable High-Speed data buffer if used in the design.	O
LINE_SYNC	Indicated the line had completed. Legacy signal, not to be used for new designs.	O
OE1	Enables the outputs of the HRC. Should be tied to ground	O
FREQ_SEL [0:1]	Frequency select bits for 120MHZ clock divider	I
120MHZ_CLK	Clock input to clock divider. This input can be up to 120 MHz.	I
DCLK_OUT	Output of 120 MHz divider	O
DMD_DCLK	This is the DDR clock used to clock data into DMD	O
DMD_TRC	Toggle rate control connected to the DMD.	O
DMD_CMD0/1	DMD Command Outputs, connect directly to DMD	O
USB_EN/	Enables the USB port.	I
VCCINT	Power supply for CMOS Internal Logic. 2.5 Volt	PWR
VCCIO1/2	Power supply for I/O. 3.3 Volt.	PWR
GNTINT	Common return for Internal Logic.	PWR
GNDIO	Common return for IO Logic	PWR

3.2 Signal Descriptions

The following section describes the requirements for the signals listed in Table 1.

3.2.1 HS_CLK

During normal operation, HS_CLK is converted to a DDR signal DMD_DCLK that is then used to clock pixel data and control data into the DMD 0.7XGA 12° DDR. Maximum operating frequency is 120MHz for HS_CLK.

3.2.2 DATA_VALID/

If RDYTOACPT is asserted, the user is free to synchronously send data to the DMD using timing provided by the HSC. All operations are completed on a line-by-line cycle. The cycle period is exactly 16 HS_CLK clocks long and begins with DATAVALID as shown in Figure 4. A minimum of one line cycle or 16 clocks of data must be sent at a time. If DATAVALID is removed, the HSC will stop loading data and stop incrementing DMD row address counters until DATAVALID goes active again. The line control bits to the HSC should be asserted and de-asserted synchronously with DATAVALID and sent 2 lines ahead of the actual DATA. DATAVALID is active LOW.

3.2.3 WRITE_EN

De-asserting the write enable flag enables the user to manipulate the address counter, without performing a write to the row being addressed. This bit must be set low during a global clear operation. WRITE_EN is active HIGH.

3.2.4 GLBCLEARMEM

The DMD will be placed in the global clear mode when GLBCLEARMEM is set high, and are clocked into the DMD. Normally, it requires 768 line loads to write to every position in the DMD. When this bit is set, it is possible to clear 16 lines at a time, thereby completing the clear operation in 1/16 the time required loading data. Separate counters are used for resetting the DMD under these conditions. This function cannot be used to load data, position the address counter, or set the device to all ones. This bit must be set at the proper value when DATAVALID transitions, and must remain asserted on subsequent lines on 16 clock cycle boundaries. See Table 2.

Table 2 Global Clear Memory						
Command	**GLBCLEARMEM**	**WRITE_EN**	**A_MODE1**	**A_MODE0**	**DATA [0:63]**	**Comments**
Line Cycle 1	1	0	1	1	X	Dummy Write
Line Cycle 2	1	0	0	1	X	Clear Line Counter
Line Cycle 3	1	0	0	1	X	Clear lines 0-15
Line Cycle 4	1	0	0	1	X	Clear lines 16-31
Line Cycle 5	1	0	0	1	X	Clear lines 32-47
Line Cycle 6	1	0	0	1	X	Clear lines 48-63
Line Cycle 50	1	0	0	1	X	Clear lines 752-767

3.2.5 A_MODE [1:0] Row Address Counter Control

A_MODE [1:0] are used to control the operation of the DMD row address counter that is used to determine the line to which DMD data is written. The counter may be cleared, set to 767, incremented, or decremented. The user must comprehend the latency, as shown in Figure 4, to coordinate the action of the control bits. Refer to Table 3 below for a description of the bit patterns. Note that the pointer will increment, decrement, set to the top or set to the bottom each time a memory cycle is performed. There is no way to hold, preset or jump the address. If a memory cycle is not active, the pointer will remain at the last position.

The DMD 0.7XGA 12° DDR does not have an automatic wrap-around row address counter (i.e. row 766,767,0,1, …). After row 767, the row address counter must be cleared to zero, to start the row address counter at Row 0.

Table 3 A Mode Bits		
A_MODE1	**A_MODE0**	**Function**
0	0	**Preset Counter to Row 767**
0	1	**Count Up (1, 2, 3…., 767)**
1	0	**Count Down (766, 765, 764 …, 0)**
1	1	**Clear Counter to Row 0**

3.2.6 TRC_IN

To reduce the data line transition frequency, a Toggle Rate Control signal TRC_IN is provided for the data inversion clocked into the DMD. When this signal is high, the TRC_IN input commands the Discovery 1100 HSC to invert the data being clocked in to the device. A low level on this signal on the TRC input specifies no data inversion. This can help in the reduction of emissions.

3.2.7 DRC_INIT_DMD

This signal from the DRC is low while the Discovery 1100 DRC initializes the DMD and the DAD. This signal is used to initialize internal registers in the HSC.

3.2.8 RDYTOACPT

When the hardware is ready to accept data via the High-Speed port, it will assert this signal. This signal is low on power-up and asserted high when initialization is complete and the high-speed port is selected.

3.2.9 Line_Sync

This is a Discovery 1000 legacy signal. It should not be used for new designs. The purpose of Line Sync was to provide a method to keep track of when each line is written. The signal would indicate when a write line sequence had completed at the end of the each line.

3.2.10 H/SPEEDBUF_EN/

This output can be used to enable data buffers to the DMD. In a system that has both USB and High Speed interface, the USB_EN needs to be pulled low to make this output active (low).

3.2.11 Output Enable 1 (OE1)

This input is the global output control for the Discovery 1100 HSC outputs. It can be used for sequencing outputs on power up as may be required by some designs. This input should be tied to ground.

3.2.12 FREQ_SEL [0.1]

As described in Section 2, the Discovery 1100 DMD HS Controller provides for frequency division of the 120MHz input reference clock to allow for the selection of operating frequencies for the DMD. The output of the divided clock is DCLK_OUT.

Table 4 Frequency Selection

FREQ_SEL1	*FREQ_SEL0*	*Frequency*
0	0	**10MHZ**
0	1	**30MHZ**
1	0	**60MHZ**
1	1	**120MHZ**

3.2.13 DCLK_OUT

This is the output from the 120MHz clock divider. It can be fed back into HS_CLK to provide the data control clock for DMD operation.

3.2.14 DMD_DCLK

This is the DMD DDR clock that connects directly to the DMD to clock in data and command information. The length of this trace should be kept as short as possible as to not add any delay to the clock and should be kept as clean as possible to prevent unwanted noise pickup.

3.2.15 DMD_CMD0/1

These signals provide commands to the DMD and should be connected directly to the corresponding DMD CMD signals. As with all signals that are routed to the DMD, trace length and attention to routing should be utmost priority to insure signal integrity.

3.2.16 USB_EN/

This signal allows for another device to control the DMD CMD signals. It is normally pulled high with a resistor, which enables the HSC to control the DMD. In typical designs, the other device that controls the DMD is a USB controller. When this line is pulled low, the DMD_DCLK and DMD CMD signals are controlled from the USBIFC. If the USB is not used, this signal must be pulled to 3.3 volts.

3.3 Typical Write Cycle

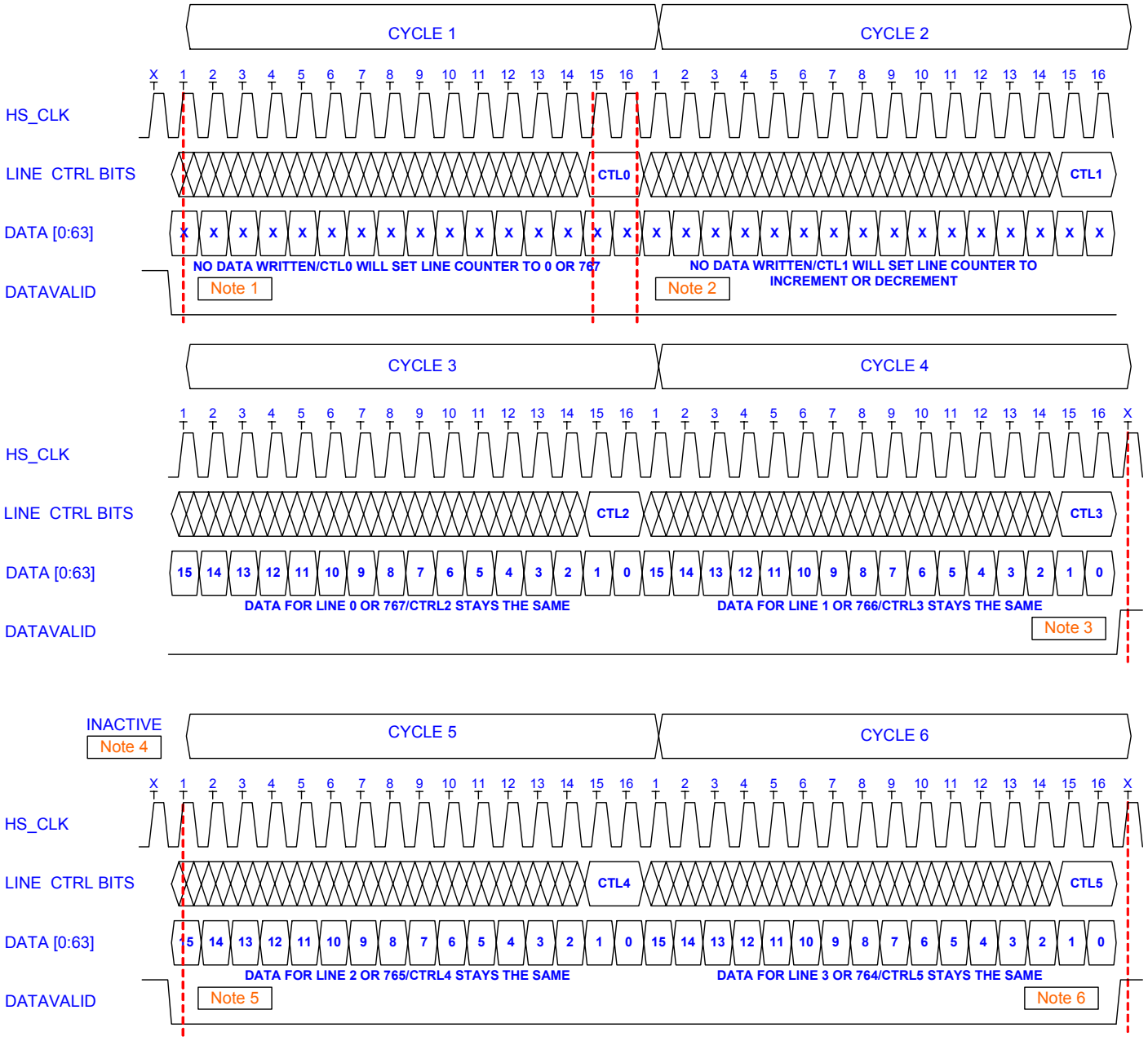


Figure 4 Data Write Cycle

Figure 4 represents a typical write cycle to the DMD where the frame is set to start at the top or bottom of the DMD and starts writing data into the DMD. This example is given to show a 2-line latency of data to the line control bits, as defined in section 2.2. The control bits that are written in one cycle are always applied to the data two cycles away. The following paragraphs give a cycle-by-cycle description of what happens in that cycle. The notes in the figure are to identify significant events. The description under the data in each cycle describes what row into which the data is being written and how the control bits for the line counter (A_MODE) are set.

Starting with cycle 1, the state of the line control bits or line counter is not known, so a dummy data write is required to set the control bits for the next line. The data bits at this point have no meaning. The line control bits need to be set during HS_CLK 15 and 16 to initialize the line counter to 0 or 767. These bits (CTL0) determine into which DMD row data is written during cycle 3. Note 1 represents the start of the write cycle and it should be noted that the DATA_VALID signal starts prior to the rising edge of the clock where the write cycle starts. See section 7 for timing details. Note 2 shows the clock cycles where the line control bits must be stable. See Figure 9 for timing requirements.

Because of the 2-line latency, a dummy data write is also required during cycle 2. The data bits for this cycle also have no meaning. The control bits set in this cycle (CTL1) for cycle 4 should then set up subsequent writes to increment or decrement the line counter. After these two cycles are complete, no data has been written to the DMD yet.

Cycle 3 is the first time data gets written into DMD memory. Depending on how the A_MODE bits were set in CTL0, the data will be written in line 0 or 767. The line control bits set in CTL1 should stay the same for the rest of the block or frame to increment or decrement.

Cycle 4 does exactly the same as cycle 3 with the exception that at Note 3; DATA_VALID is set high right after clock 16, but before the rising edge of the next clock. This is shown in this example to show that writing data to the DMD can be stopped and started while writing a block or frame. This is useful for designs that have limited size buffers and can't maintain a continuous flow of data to the DMD. Note 4 represents a period of inactivity. The control signals (CTL2) latched in at cycle 3 will apply to the next cycle when DATA_VALID is reasserted.

Cycle 5 starts the write cycle to the next line, which should be line 2 or 765. The same timing for DATA_VALID as for cycle 1 is applicable here. DATA_VALID goes high at note 6 to indicate the end of the write cycle for this example. It should be noted that 6 cycles have been required and only four lines of data have been written. If the DMD is used in a continuous write mode, at the last line of data written, the A_MODE bits should be set to reset the counter to 0 or 767 so no extra cycle will be needed.

The end result is that to write the entire frame it would write 770 lines, 2 dummy lines at the beginning to latch in line control bit and the set the line counter to start or end of the frame, then 768 lines of data. Refer to Figure 8 for detailed timing information.

4 Layout Guidelines

4.1 Overview

The Discovery DDC1100 component set provides a highly integrated, high performance DMD solution that enables designers to create small size, high data rate products. The component set, when implemented with the reference material provided, provides all the electronics required to drive and control the DMD sub system on a small PWB depending on configuration

The majority of the circuitry in the DDC1100 reference design is high-speed digital. High-speed digital circuitry includes a 64 bit input data interface, and an HRC (high-speed controller) to DMD interface. Proper layout of the high-speed digital and analog circuits is critical to insure a working and robust design.

Items covered in this section deal mainly with the HSC. See the DDC1100 Controller Board TRM for a system overview.

4.2 High Speed Signals

In addition to the oscillator circuit, most signals are either 60 MHz to 120 MHz. The output switching times are very fast and care should be used to prevent ring, reflections and cross talk. High-speed design techniques should be used with these signals. It is recommended that termination resistors be placed close to these output pins and trace length of these signal be keep short and as close to the same length as possible. It is suggested that high-speed signals maintain a trace impedance of 50 ohms.

4.3 Oscillators

The HSC utilizes oscillators for the DAD interface. PSI recommends PI filters on the power entry to the oscillators as an EMI precaution. The PI filter capacitor on the oscillator side should be located as close to the oscillator's supply pin as possible. The series termination resistor on the oscillator clock output should be located close to the output pin on the oscillator. Having a surface ground plane under the oscillator package can reduce EMI radiation. The surface ground plane should be tied to the internal ground planes with multiple vias.

4.4 DC Supply Voltages

The HSC electronics requires DC supply voltages of 2.5V, 3.3V. PSI recommends filtering these supply voltages with PI filters. The PI filters should be located at the power entry to the PWB. Trace widths for the supply voltages and ground connections should be sized based current and desired temperature rise in accordance with a standard such as IPC-2221.

4.5 Decoupling Capacitors

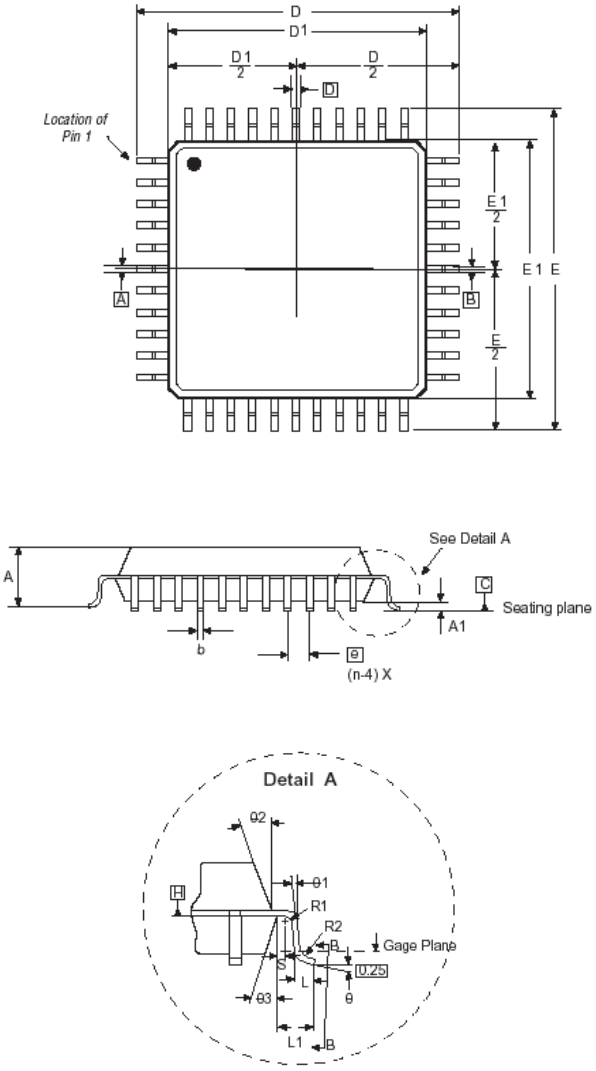
Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. PSI recommends the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located very close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1". Otherwise the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1" to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

5 Device Packaging Information

5.1 Pin Diagram

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min	**Nom.**	**Max**
A	-	-	1.27
A1	0.05	-	-
b	0.30	0.37	0.45
D	11.75	-	12.25
D1	9.90	-	10.10
e	0.80 BSC		
E	11.75	-	12.25
E1	9.90	-	10.10
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
N	44		



Notes:

1. All dimensions and tolerances conform to ANSI Y14.5 – 1994
2. Controlling dimensions: millimeters.
3. JEDEC reference MS-029 option FA-1.

Figure 5 Pin Package Diagram

5.2 Packaging Information

Table 5 Package Information	
Description	**Specification**
Ordering Code Reference	T
Packaging Acronym	TQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-026
JEDEC Option	BCB
Maximum Lead Coplanarity	0.004 inches (0.01 mm)
Weight	0.3g

5.3 Packaging Dimension Formats & Units

Package outline dimensions are shown in the following formats:

Table 6 Package Outline Units	
Unit	**Description**
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates square feature for a package with equal length and width dimensions.

5.4 Schematic Symbol

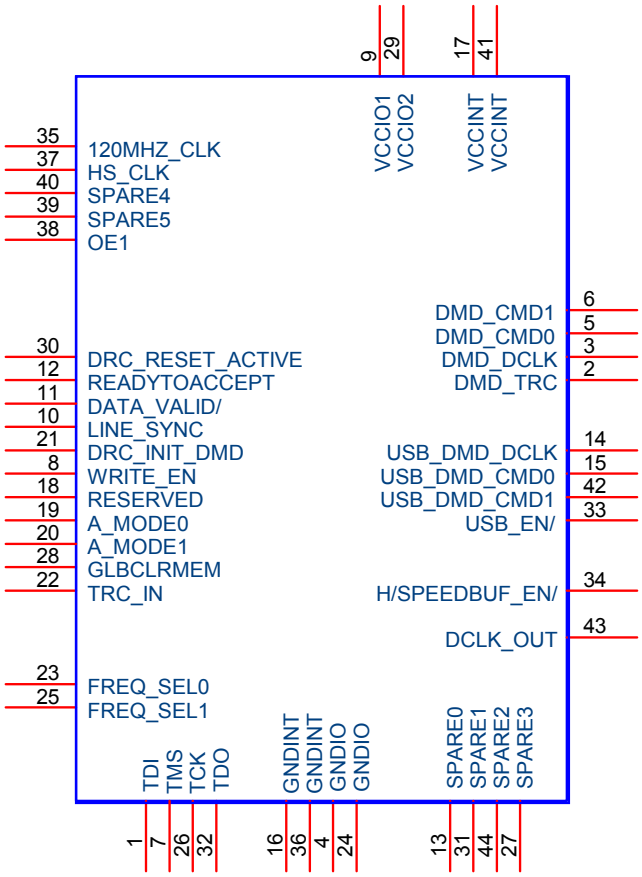


Figure 6 High Speed Controller Schematic Symbol

6 General Electrical Requirements

6.1 Absolute Maximum Ratings

Table 7 Absolute Maximum Ratings

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage	With respect to ground	-0.5	3.6	V
V_{CCIO}	Supply voltage		-0.5	3.6	V
V_I	DC input voltage	*(1)*	-2.0	4.6	V
I_{OUT}	DC output current, per pin		-33	50	mA
T_{SIG}	Storage temperature	No bias	-65	150	° C
T_A	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	Under bias	-65	135	° C

6.2 Recommended Operating Conditions

Table 8 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CCINT}	Supply voltage for internal logic and input buffers		3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(2)*	-0.5	3.9	V
V_O	Output voltage	Under bias	0	V_{CCIO}	V
T_A	Ambient temperature		0	70	° C
T_J	Junction temperature		0	90	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

6.3 Device DC Operating Conditions

Table 9 Device DC Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage for 3.3-V TTL/CMOS		2.0	3.9	V
V_{IL}	Low-level input voltage for 3.3-V TTL/CMOS and PCI compliance		–0.5	0.8	V
V_{OH}	3.3-V high-level CMOS output voltage	IOH = –0.1 mA DC, VCCIO = 3.00 V *(3)*	V_{CCIO} - 0.2		V
V_{OL}	3.3-V low-level CMOS output voltage	IOL = 0.1 mA DC, VCCIO = 3.00 V *(4)*		0.2	V
I_I	Input leakage current	current VI = –0.5 to 3.9 V *(5)*	-10	10	uA
I_{OZ}	Tri-state output off-state current	VI = –0.5 to 3.9 V *(5)*	-10	10	uA

Notes to tables:

Note 1 Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Note 2 All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before VCCINT and VCCIO are powered.

Note 3 The parameter is measured with 50% of the outputs each sourcing the specified current. The I OH parameter refers to high-level TTL or CMOS output current.

Note 4 The parameter is measured with 50% of the outputs each sinking the specified current. The I OL parameter refers to low-level TTL or CMOS output current.

Note 5 This value is specified for normal device operation. The maximum leakage current during power-up is ±300 µA.

7 TIMING CHARACTERISTICS

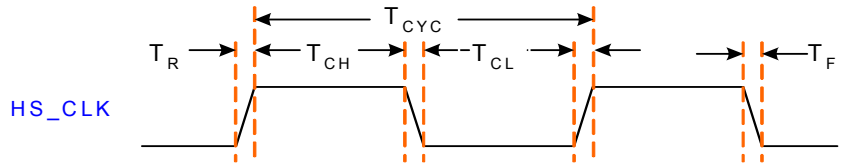


Figure 7 HS_CLK Timing

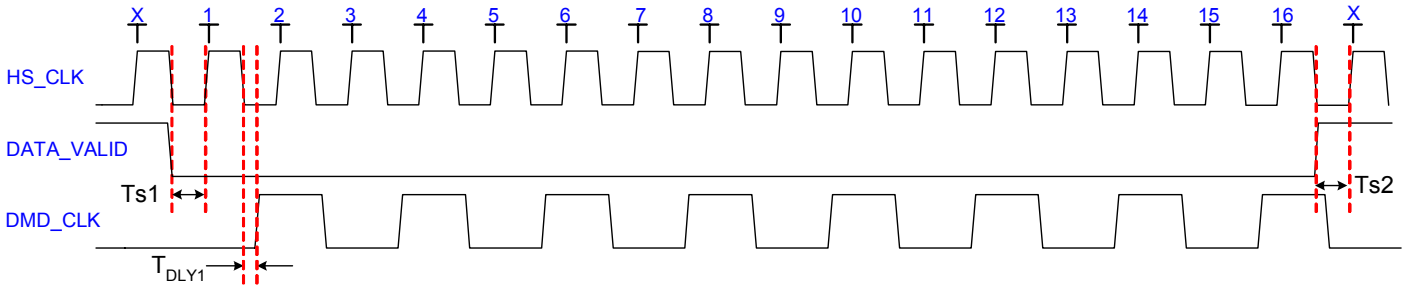


Figure 8 HS_CLK to Data Valid to DMD_DCLK timing

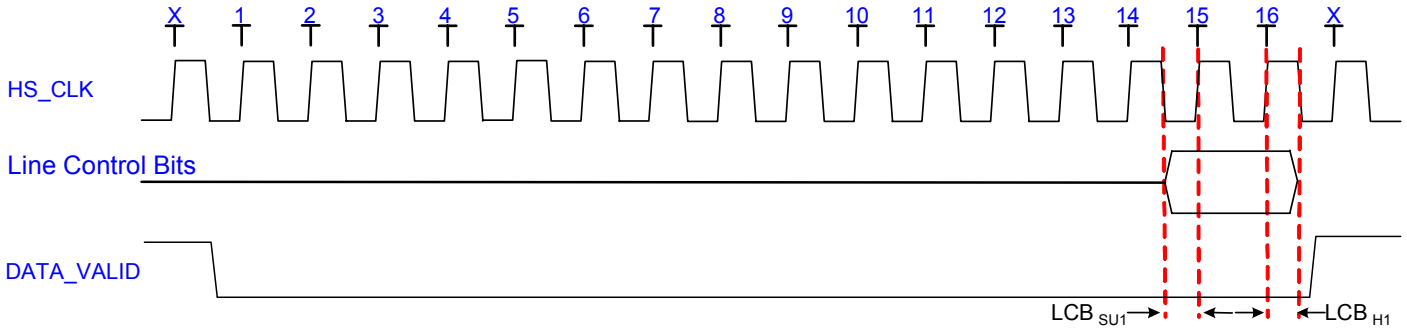


Figure 9 Line Control Bits setup and hold requirements

7.1 Critical Timing Characteristics

Table 10 Critical Timing Characteristics				
Symbol	**Parameter**	**Min**	**Max**	**Unit**
Ts1	DATA_VALID Setup Time - start of cycle before rising edge of HS_CLK (note 1)	3.0	6.0	ns
Ts2	DATA_VALID Disable Time - end of cycle before rising edge of start of next cycle (note 1)	3.0	6.0	ns
Tdly1	HS_CLK falling edge to DMD_DCLK delay		2.4	ns
LCB_{SU1}	Line control bits setup time before clock 15	5		ns
LCB_{H1}	Line control bits hold time after clock 16	5		ns
Tcyc	HS_CLK period (note 2)	8.33		ns
Tch/Tcl	HS_CLK high/low time (note 2)	3.75	4.58	ns
Tr/Tf	HS_CLK rise/fall time (note 2)		1	ns

Note 1 Ts1 and Ts2 max times are for 120 MHz operation. As the frequency lowers, the max time can increase to 70% of the period of the frequency used.

Note 2 For frequencies in the range of up to 120MHz a 45/55 duty cycle oscillator is required to meet setup and hold times.

8 Discovery 1100 HS DMD Controller Pin Map

Table 11 Discovery 1100 HS DMD Controller Pin Map

NAME	I/O	DESCRIPTION	CONNECT TO	PIN#
TDI	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	1
DMD_TRC	O	Selects to invert or not invert DMD data	DMD PIN L1	2
DMD_DCLK	O	DMD DDR Clock, used to clock data into DMD	DMD PIN C15	3
GNDIO	P	GND	GROUND	4
DMD_CMD0	O	DMD Control – to DMD	DMD PIN B18	5
DMD_CMD1	O	DMD Control – to DMD	DMD PIN N3	6
TMS	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	7
WRITE_EN	I	Indicates to DMD whether data is written	USER INPUT	8
VCCIO1	P	VCC I/O 3.3V	3.3 VOLT	9
LINE_SYNC	O	Indicates that a line has been completed	USER OUTPUT	10
DATA_VALID/	I	Starts a DMD data write cycle	USER INPUT	11
READYTOACCEPT	O	Indicates DMD is Ready to Accept data	USER OUTPUT	12
SPARE0	I	Currently unused		13
USB_CLK	I	DMD DDR CLK – From USB Controller	USBIFC PIN 132	14
USB_DMD_CMD0	I	DMD Control – From USB Controller	USBIFC PIN 133	15
GNDINT	P	GND	GROUND	16
VCCINT	P	Internal VCC 2.5V	2.5 VOLT	17
Reserved	I	Reserved	See Note 2	18
A_MODE0	I	DMD A_Mode0	USER INPUT	19
A_MODE1	I	DMD A_Mode1	USER INPUT	20
DRC_INIT_DMD	I	DRC_INIT_DMD	DRC PIN 28	21
TRC_IN	I	HS_TRC	USER INPUT	22
FREQ_SEL0	I	Frequency Select	USER INPUT	23
GNDIO	P	GND	GROUND	24
FREQ_SEL1	I	Frequency Select	USER INPUT	25
TCK	I	JTAG – Pull down with 1k ohm to ground.	See Note 1	26
SPARE3	O	Drives LED to indicate Parallel Port Enabled		27
GLBCLRMEM	I	Global clear Memory (See Note 2)	USER INPUT	28
VCCIO2	P	VCC I/O 3.3V	3.3 VOLT	29
DRC_RESET_ACTIVE	I	Indicates a Reset is active	DRC PIN 1	30
SPARE1	I	Currently unused		31
TDO	O	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	32
USB_EN/	I	Select USB control	USBIFC PIN 136	33
H/SPEEDBUF_EN/	O	Enables high speed data path buffers	USER OUTPUT	34
120MHZ_CLK	I	120 MHZ on board clock	USER INPUT	35
GNDINT	P	GND	GROUND	36
HS_CLK	I	SDR Data Clock used to generate DMD DDR Clock	USER INPUT	37
OE1	I	Enables HSC Outputs	GROUND	38
SPARE5	I	Unused		39
SPARE4	I	Unused		40
VCCINT	P	Internal VCC 2.5V	2.5 VOLT	41
USB_DMD_CMD1	I	DMD Control - From USB Controller	USBIFC PIN 134	42
DCLK_OUT	O	SDR Clock that can be used to generate DMD HS_CLK	USER OUTPUT	43
SPARE2	I	Unused		44

Note 1. User may bring these signals to a connector for possible Future use. The programmed contents of this device are protected from being changed or duplicated. Use of these signals to change the programmed contents of this device could damage the HSC and the DMD and void the warranty.

Note 2. For HSC Rev B (Revision may be unmarked.) pin 18 should be tied to GBLCLRMEM (pin 28). For HSC Rev D (released August, 2004) pin 18 is not used, but may be used for future revisions.

9 ACRONYMS

DAD 1000 DMD Power and Reset Driver

DDR Double Data Rate

SDR Single Data Rate

DMD Digital Micromirror Device

GUI Graphical User Interface

USB Universal Serial Bus

DRC DAD Reset Controller

HSC High-speed Controller

HSP High-Speed Port

USBIFC USB Interface Controller

SCP Serial Communications Port

CDS Customer Data Sheet