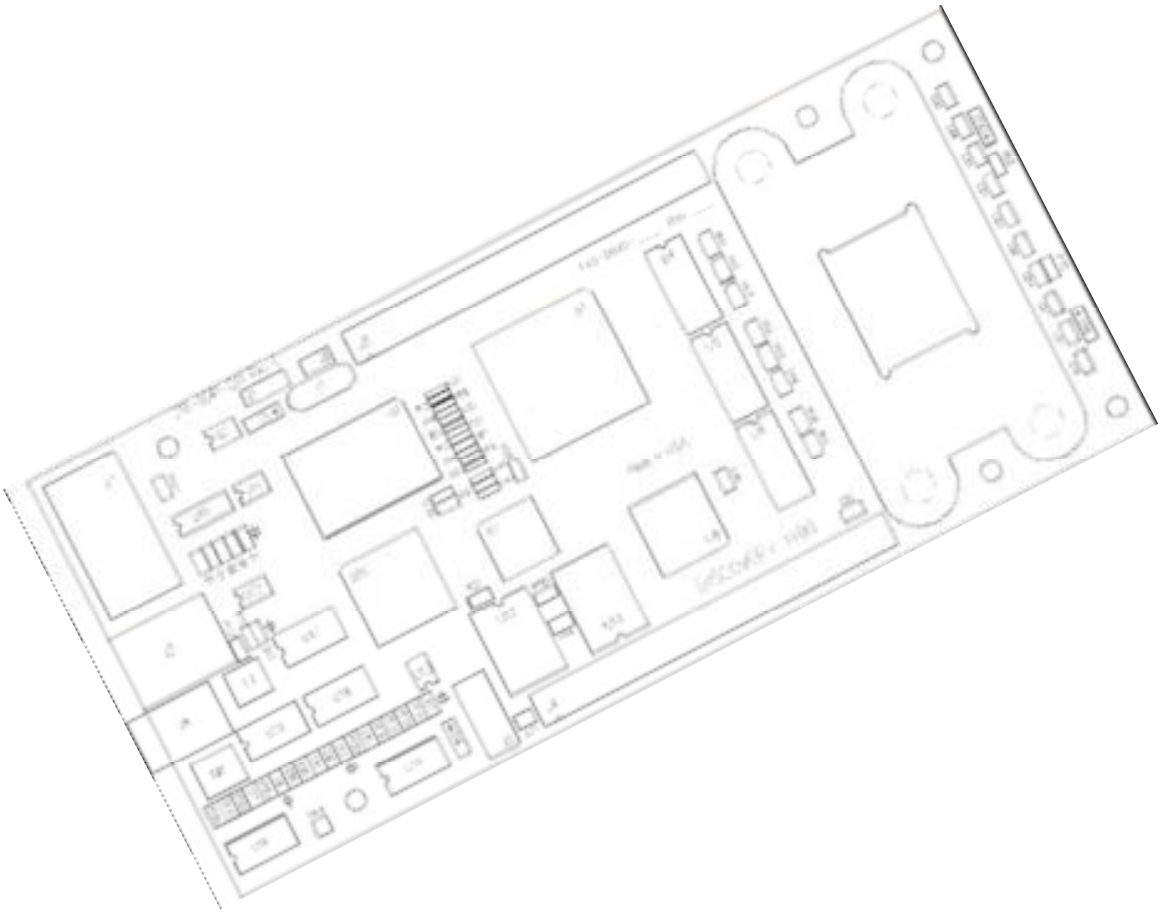
Reference Manual
TI DN 2506023 REV A
Ocotber 2004

Discovery™ 1100 PWB Layout Guidelines

This document provides recommendations for component placement and signal routing for the Discovery 1100 Controller Board reference design.



Revisions		
Rev	Descriptions	Date
TI 2506023 A	Changed to TI drawing number system (Applicable Documents 2.0)	10/4/04

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1.0 Scope

This document provides recommendations for component placement and signal routing for the Discovery Controller Board (DCB) reference design.

2.0 Applicable Documents

- DMD .7 XGA DDR Discovery User Data Sheet, TI DN 2503884
- DAD1000 Power and Reset Driver Discovery User Data Sheet, TI DN 2503885
- Discovery 1100 HSC Customer Data Sheet, TI DN 2506019
- Discovery 1100 DRC Customer Data Sheet, TI DN 2506020
- Discovery 1100 USBIF Customer Data Sheet, TI DN 2506018
- Discovery 1100 Controller Board & Starter Kit Technical Reference Manual,

  TI DN 250606
- Mechanical Drawings – Digital Micromirror Device (DMD), Controller Board, mounting diagrams

3.0 Introduction

It is assumed that reference design will be implemented on a single multi-layer printed wiring board (PWB) with adequate power and ground planes. A target impedance of 50 ohm is assumed for all signal layers. Other impedances can be used, but termination values must be adjusted.

4.0 PWB Characteristics

4.1 PWB Stack up

There are many possibilities for the number of PWB layers and the stack up of the layers. The PWB stack up should incorporate the Discovery 1100 guidelines as well as the other requirements of the Discovery 1100 Chipset. Two to three internal strip line layers are required for the Discovery 1100 signals. At least one of the plane layers adjacent to each of the two Discovery 1100 signal layers should be a solid ground plane. TI recommends providing a solid plane for the 3.3V and DMD VCC power planes. A suggested layer stack up is listed in Table 1.

Table 1. DCB Reference PWB Layer Stack-Up

Layer No.	*Layer Name*
1	**Top Components and Signal Routing**
2	**Power Plane**
3	**Signal Routing**
4	**Ground Plane**
5	**Signal Routing**
6	**Signal Routing**
7	**Ground Plane**
8	**Bottom Components and Signal Routing**

4.2 Trace Impedance

The data signal traces should be designed for controlled impedance.

4.3 Power Planes

TI recommends solid planes for ground, 3.3V and DMD VCC. For the Discovery DMD PWB, the 3.3V plane can be split with DCB VCC. If split voltage planes are used, then high-speed signals on adjacent layers should not cross the split in the plane.

Care must be taken to not create slots in the power and ground planes. Vias should not be placed so the anti-pads on the plane layers overlap.

4.4 Plating

TI recommends the DMD pads be plated with a minimum of 30uin of electrolytic gold over a minimum of 150uin of electrolytic nickel. While other plating materials are possible, TI recommends non DMD pads be plated with 5-15uin of electrolytic gold over a minimum of 150uin of electrolytic nickel.

5.0 DC Supply Voltages

The Discovery 1100 DMD electronics require DC supply voltages of 3.3V, 5.0V and 12V. TI recommends filtering these supply voltages with PI filters as shown in the reference design. The PI filters should be located at the power entry to the PWB. Trace widths for the supply voltages and ground connections should be sized based current and desired temperature rise in accordance with a standard such as IPC-2221.

6.0 Digital Controller Board

6.1 Discovery 1100 DMD Decoupling

General decoupling capacitors for the Discovery 1100 DMD should be distributed around the DCB and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly to the ground and power planes. The power and ground pads of the Discovery 1100 DMD should be tied to the voltage and ground planes with their own vias.

6.2 DMD Interface

The digital interface from the HSC and data interface to the DMD runs at clock rates up to 60MHz. Data is clocked into the DMD on both the rising and falling edge of the clock, so effectively the interface runs at 120MHz. The high-speed signals should all be kept as short as possible with series termination resistors as close to the driver as possible. Also reference the DMD datasheet for timing information.

Trace length matching requirements will be a function of the driving IC and the Discovery Chipset timing parameters (See Discovery 1100 Technical Reference Manual (TRM)).

6.3 Oscillators and Crystals

The Discovery 1100 reference design utilizes two oscillators. TI recommends PI filters on the power entry to the oscillators as an EMI precaution. The PI filter capacitor on the oscillator side should be located as close to the oscillator's supply pin as possible.

Having a surface ground plane under the oscillator or crystal package can reduce EMI radiation. The surface ground plane should be tied to the internal ground planes with multiple vias.

6.4 Trace Length Matching

The Discovery 1100 DMD data signals require precise length matching. It is important that the propagation delays are matched. The signals should be matched in length to at least +/-5mil relative. Matching all signals exactly will maximize the channel margin.

6.5 VCC

The VCC pins of the 0.7XGA should be connected directly to the DMD VCC plane. Decoupling for the VCC should be distributed around the DMD and placed to minimize the distance from the voltage and ground pads. Each decoupling capacitor should have vias directly connected to the ground and power planes. The VCC and GND pads of the DMD should be tied to the VCC and ground planes with their own vias.

6.6 VCC2

The VCC2 voltage can be routed to the DMD as a trace. Decoupling capacitors should be placed to minimize the distance from the DMD's VCC2 and ground pads. Using wide etch from the decoupling capacitors to the DMD connection will reduce inductance and improve decoupling performance.

6.7 DMD Layout

See the DMD customer datasheet and mechanical ICD for package dimensions, timing and pin out information. Also, see the reference design board interface drawings for PWB layout recommendations.

7.0 DMD Drive Voltage Generation

7.1 DAD1000

The DAD1000 generates the RESET voltages for the DMD. The DMD drive outputs from the DAD1000 (OUT[15:0]) should be routed with minimum trace width of 11mil and a minimum spacing of 15mil. The Vbias, Vrst and VCC2 traces from the output capacitors to the DAD1000 should also be routed with a minimum trace width and spacing of 11mil and 15mil, respectively. See the DAD1000 customer datasheet for mechanical package and layout information.

8.0 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component. It is recommended that the placement of and routing for the decoupling capacitors meet the following guidelines:

- The supply voltage pin of the capacitor should be located very close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1 inch. Otherwise, the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1 inch to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.