Customer Data Sheet
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April 2005

Discovery™ 1100 USBIFC (USB Interface Controller)

This manual covers the functionality of the Discovery 1100 USBIFC (USB Interface Controller) component. When the USB port is used the Discovery 1100 USBIFC provides the DMD mirror reset and timing information to the DAD1000 and DMD

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Revisions

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717-0040-003 B	Complete rewrite with more detailed design information	1/7/04
717-0040-003 C	Corrected mechanical information	1/23/04
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1 Overview

This document covers the functionality of the Discovery 1100 USBIFC (USB Interface Controller) component. When the USB port is used the Discovery 1100 USBIFC provides the DMD mirror reset and timing information to the DAD1000 and DMD.

Shown below are two simplified block diagrams showing the use of the USBIFC with and without the HSC.

The block diagram in Figure 1 is a typical system using both high-speed (HS) and USB interfaces. The end-user may control the DMD from either the USB or HS interface. When the USB port is used the DMD mirror resets are initiated through the USB interface and passed to the DRC through the USB support components. The DRC provides the reset logic required for the DAD1000 to drive the DMD mirror reset inputs.

The six components shown are:

DMD 0.7XGA 12^{o} DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver
Cypress FX2 – 2.0 USB controller
Discovery 1100 USBIFC (USB Interface Controller) – provides interface between USB and DMD components
Discovery 1100 DRC (DAD RESET Controller) – provides reset interface to DAD and DMD
Discovery 1100 HSC (HS Controller) – provides high-speed clock control and command interface

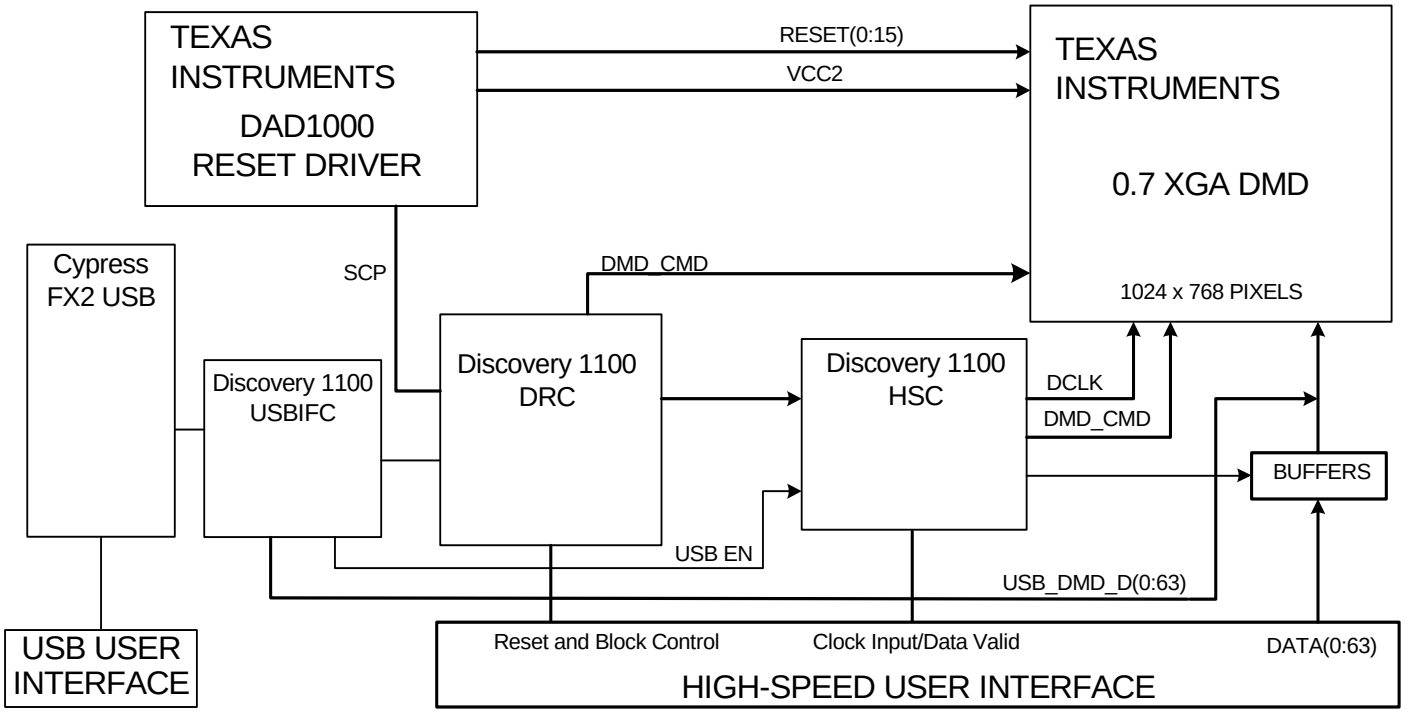

Figure 1 Discovery Block Diagram with USB

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The second block diagram shown in Figure 2 shows typical system with USB only interface.

The four components shown are:

DMD 0.7XGA 12° DMD Discovery – Spatial Light Modulator
DAD1000 – DMD reset driver
Discovery 1100 DRC (DAD RESET Controller) – provides reset interface to DAD and DMD
Discovery 1100 USBIFC (USB Interface Controller) – provides clock control and command interface

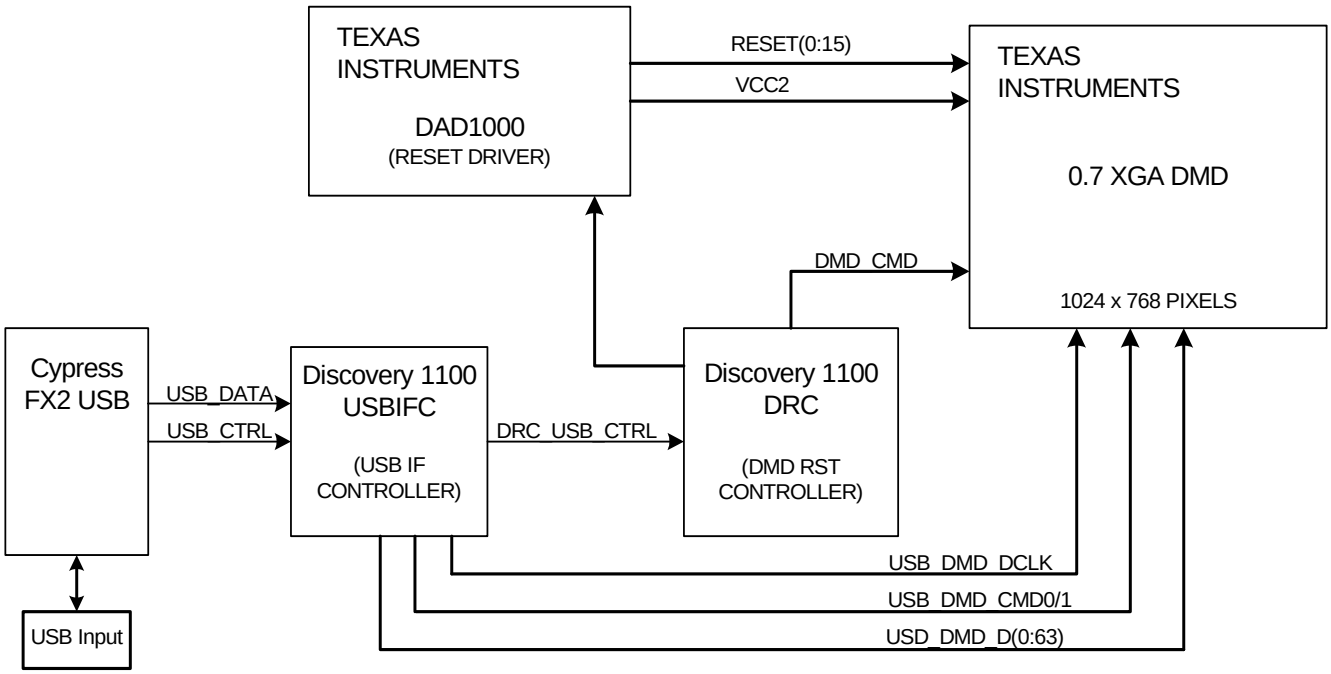

Figure 2 Discovery Block Diagram without HSC

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2 FUNCTIONAL DESCRIPTION

The Discovery 1100 USBIFC is designed to work with the Cypress FX2 USB controller to provide USB 2.0 functionality for the Discovery 1100. The combination of these chips provides the ability to operate the Discovery 1100 at 100 frames per second. With these chips along with the DRC, all of the logic necessary to control the DMD and DAD1000 devices can be combined to provide a small footprint low speed system.

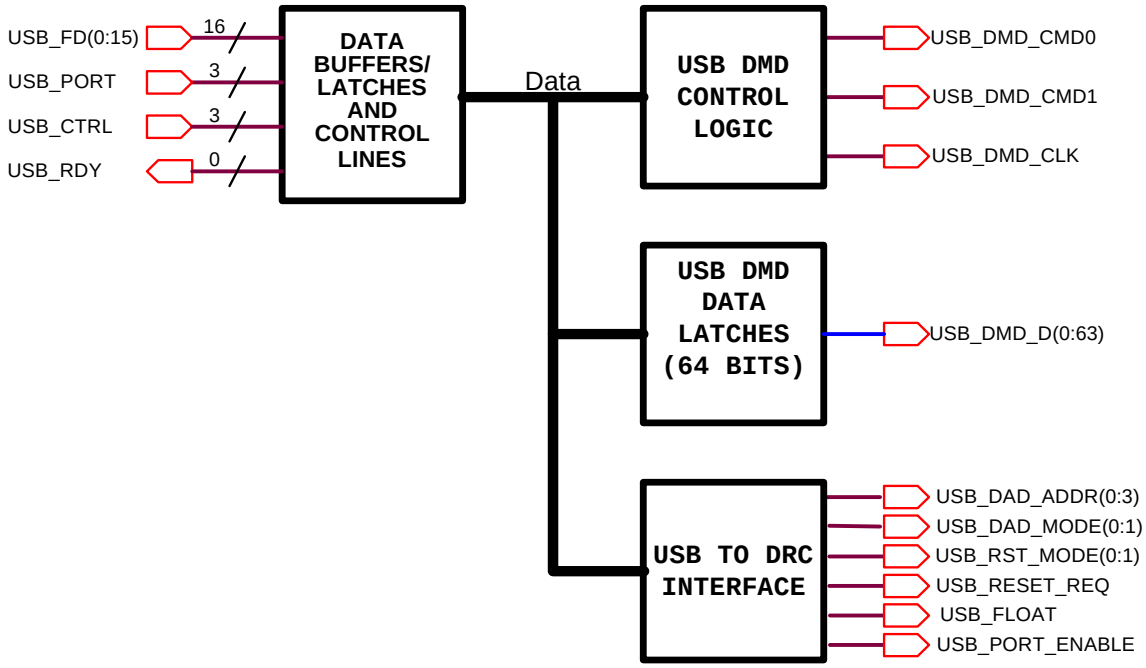

Figure 3 USBIFC Block Diagram

The I/O from the USB controller chip is divided into four functional sections.

2.1 Data Buffers/Latches and Control Lines

The Discovery 1100 USBIFC is connected to the Cypress FX2 USB 2.0 16 bit data bus and several control lines to provide the USB interface. The FX2 consists of several components, SIE (serial interface engine), a micro controller and a 16-bit data and control interface. The single 16-bit data bus provides data to latches in the USBIFC used for DMD data and control bits to operate the DMD. A typical sequence starts with the FX2 sending a command to latch line control bits followed by a data stream to be stored in the DMD memory, followed by a command to reset the DMD.

The FX2 provides the SIE that handles the raw USB data. The SIE handles all error conditions and will not be placed into endpoint buffers unless the data is valid. When valid data comes in to the SIE, it is placed in either FX2 endpoint buffer 0 (commands) or endpoint buffer 2 (data). Endpoint buffer 0 receives information to set up the USBIFC to control the DRC and the DMD through the HSC or the DMD directly and endpoint buffer 2 only has image data, When data comes into endpoint buffer 0, the micro controller will set up the FX2 to execute the requested command. When data comes in endpoint buffer 2, the data is automatically transferred into the DMD by the logic in he FX2 and USBIFC.

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2.2 USB DMD Control Logic

When operating in USB mode, this section provides all the logic and timing for transferring data into the DMD data memory. These signals go to the HSC when a system has both USB and a high-speed port. If the system only has USB, these signals go directly to the DMD.

2.3 USB DMD Data Latches

Since the data bus between the FX2 and USBIFC is only 16 bits, data is sent over 16 bits at a time and latched into 4 16-bit latches. When the data is latched into the forth latch, the USB_DMD_DCLK is generated to latch the data into the DMD memory.

2.4 USB to DRC Interface

The USB controller controls the DAD1000 through the DRC. The control signals are used to provide the required control for the DAD.

Commands from the USB processor are routed to the USB controller via a 16-bit bus. The processor links commands delivered via the USB connection to the Discovery system. User commands are used to control and initialize both the DMD and the DAD1000 devices.

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3 PIN FUNCTIONAL DESCRIPTION

The functions listed are for information purpose only. The designer has no real access to any of these pins and all control is handled by the FX2 USB controller the ActiveX controls. Refer to 715-0040-001, Discovery 1100 Controller Board GUI User's & Programmers Guide. Most of this information is also duplicated in the HSC, DRC and Controller Board TRM.

Table 1 Pin Functional Description

NAME	DESCRIPTION	I/O
USB_FD (0:15)	Data from USB chip with series termination	I
USB_DMD_D (0:63)	Data to DMD with series termination	O
USB_DAD_ADDR (0:3)	USB DAD Reset Block address select	O
USB_DAD_MODE (0:1)	USB DAD Mode Select	O
USB_DMD_CLK	DMD DDR CLOCK	O
USB_RST_MODE (0:1)	USB Reset mode selection	I
USB_DMD_CMD0/1	DMD Command outputs. Connects to HSC and/or DMD	O
USB_PORT_EN	USB Port Enable	O
VCCIO1	VCC IO 3.3V	P
VCCIO2	VCC IO 3.3V	P
VCCINT	VCC IO 2.5V	P
GND	GND	P

3.1 USB_DMD_D (00:63)

The data interface to the DMD is via 64 data lines. The FX2 send 4 16-bit words to the USBIFC and then the USBIFC clocks the data into the DMD with the USB_DMD_CLK signal. This is repeated 16 times to load one line of data. The user must load a minimum of one line per transaction. The entire process is handled by the USBIFC.

3.2 USB_FD [0:15]

The FX2 and USBIFC pass all data through this 16 bit wide FIFO interface. The FX2 is set up with 4 512-byte buffers so data transfer can operate without any throttle control required. In a typical cycle, line control bits will be sent across this bus and latched, then the data for the DMD will be transferred in blocks.

3.3 USB_DAD_ADDR (0:3) and USB_DAD_MODE (0:1)

These bits allow the selection of which block or groups of blocks will be reset. Refer to the DRC CDS (714-0040-002) for detailed description of how these bits are used.

3.4 USB_DMD_DCLK

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This is the USB DMD DDR clock that connects to the HSC or DMD to clock in data and command information. The length of this trace should be kept as short as possible as to not add any delay to the clock and should be kept as clean as possible to prevent unwanted noise pickup.

3.5 USB_RST_MODE (0:1)

These signals should be connected directly to the USB_RSTMODE(0,1) signals on the DRC. The two signals are always low to enable direct reset.

3.6 USB_DMD_CMD0/1

These signals provide commands to the DMD and should be connected directly to the corresponding DMD CMD signals through the HSC or directly to the DMD. As with all signals that are routed to the DMD, trace length and attention to routing should be utmost priority to insure signal integrity.

3.7 USB_PORT_EN

USB_PORT_EN is controlled by the firmware in the Cypress FX2 USB controller. If the FX2 USB has been connected to a system and communication between the system and the FX2 has been established, then the USB_PORT_EN will be enabled. This signal can be used in systems with a high-speed port to disable the high-speed section.

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4 Layout Guidelines

4.1 Overview

The Discovery DDC1100 component set provides a highly integrated, high performance DMD solution that enables designers to create small size, high data rate products. The component set, when implemented with the reference material provided, provides all the electronics required to drive and control the DMD sub system on a small PWB depending on configuration

The majority of the circuitry in the DDC1100 reference design is high-speed digital. High-speed digital circuitry includes a 64 bit input data interface, and an HRC (high-speed controller) to DMD interface. Proper layout of the high-speed digital and analog circuits is critical to insure a working and robust design.

Items covered in this section deal mainly with the USBIFC. See the DDC1100 Controller Board TRM for a system overview.

4.2 High Speed Signals

Data transfer between the USB Controller and the USBIFC is at 48 MHz. This speed allows the designer some flexibility in component placement.

The USB physical interface is running at 480 Mbps, so considerable care must be taken in routing and controlling Impedance and crosstalk. In addition to referencing the USB Specification Revision 2.0, Cypress Semiconductors have 2 application notes that should be referenced, EZ-USB FX2™ PCB Design Recommendations and High-speed USB PCB Layout Recommendations

4.3 DC Supply Voltages

The USBIFC electronics requires DC supply voltages of 2.5V, 3.3V. TI recommends filtering these supply voltages with PI filters. The PI filters should be located at the power entry to the PWB. Trace widths for the supply voltages and ground connections should be sized based on current and desired temperature rise in accordance with a standard such as IPC-2221.

4.4 Decoupling Capacitors

Decoupling capacitors should be placed to minimize the distance from the decoupling capacitor to the supply and ground pin of the component.

- The supply voltage pin of the capacitor should be located very close to the device supply voltage pin(s). The decoupling capacitor should have vias to ground and voltage planes. The device can be connected directly to the decoupling capacitor (no via) if the trace length is less than 0.1”. Otherwise the component should be tied to the voltage or ground plane through separate vias.
- The trace lengths of the voltage and ground connections for decoupling capacitors and components should be less than 0.1” to minimize inductance.
- The trace width of the power and ground connection to decoupling capacitors and components should be as wide as possible to minimize inductance.
- Connecting decoupling capacitors to ground and power planes through multiple vias can reduce inductance and improve noise performance.
- Decoupling performance can be improved by utilizing low ESR and low ESL capacitors.

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5 DEVICE PACKAGING INFORMATION

5.1 Pin Diagram

Package Outline Figure Reference			
Symbol	**Millimeters**		
	Min	**Nom.**	**Max**
A	-	-	1.60
A1	0.05	-	0.15
b	0.17	0.22	0.27
D	22.00 BSC		
D1	20.00 BSC		
e	0.50 BSC		
E	22.00 BSC		
E1	20.00 BSC		
θ	0°	3.5°	7°
θ1	0°	-	-
θ2	11°	12°	13°
θ3	11°	12°	13°
L	0.45	0.60	0.75
L1	1.00 REF		
R1	0.08	-	-
R2	0.08	-	0.20
S	0.20	-	-
N	144		

Notes:

1. **All dimensions and tolerances conform to ANSI Y14.5 – 1994**
2. **Controlling dimensions: millimeters.**
3. **JEDEC reference MS-029 option FA-1.**

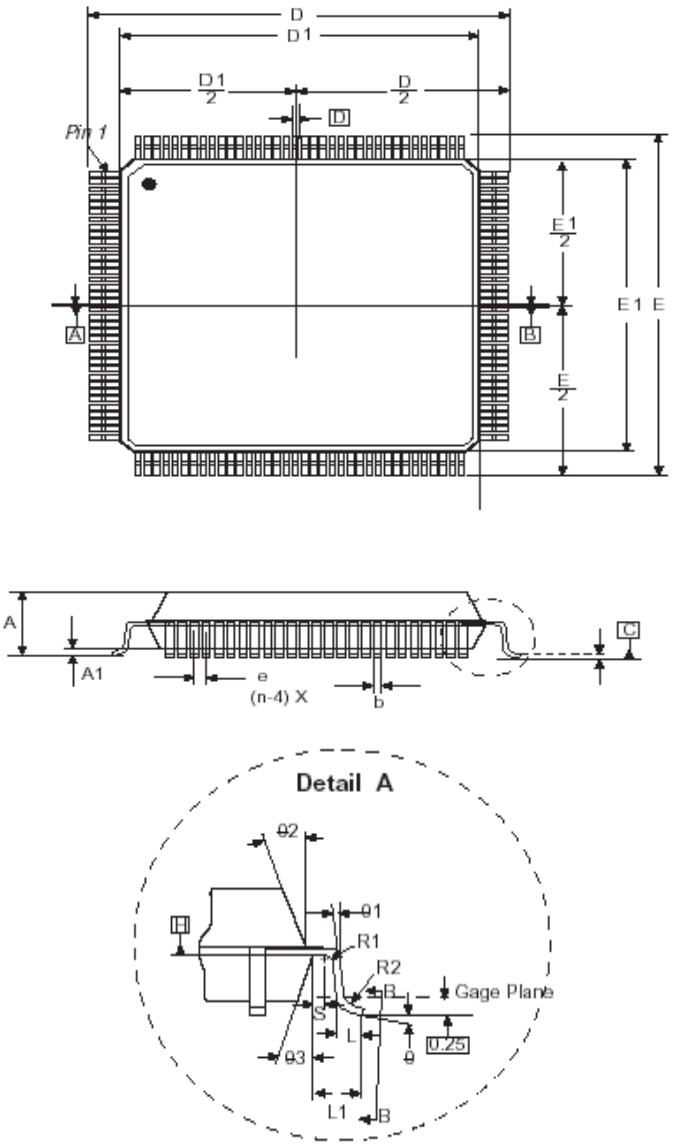

Figure 4 Package Mechanical Layout

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5.2 Packaging Information

Table 2 Package Information	
PACKAGE INFORMATION	
Package Acronym	PQFP
Lead Material	Copper
Lead Finish	Solder plate (85/15 typical)
JEDEC Outline	MS-029
JEDEC Option	FA-1
Maximum Lead Coplanarity	0.003 inches (0.08 mm)
Weight	5.7 g
Moisture Sensitivity Level	Printed on moisture barrier bag

5.3 Packaging Dimension Formats & Units

Table 3 Package Outline Units	
Unit	**Description**
BSC	Basic. Represents theoretical exact dimension or dimension target.
Min.	Minimum dimension specified.
Max.	Maximum dimension specified.
Ref.	Reference. Represents dimension for reference use only. This value is not a device specification.
Typ.	Typical. Provided as a general value. This value is not a device specification.
R	Radius. Represents curve dimension.
Dia.	Diameter. Represents curve dimension.
Sq.	Square. Indicates square feature for a package with equal length and width dimensions.

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5.4 Part Symbol

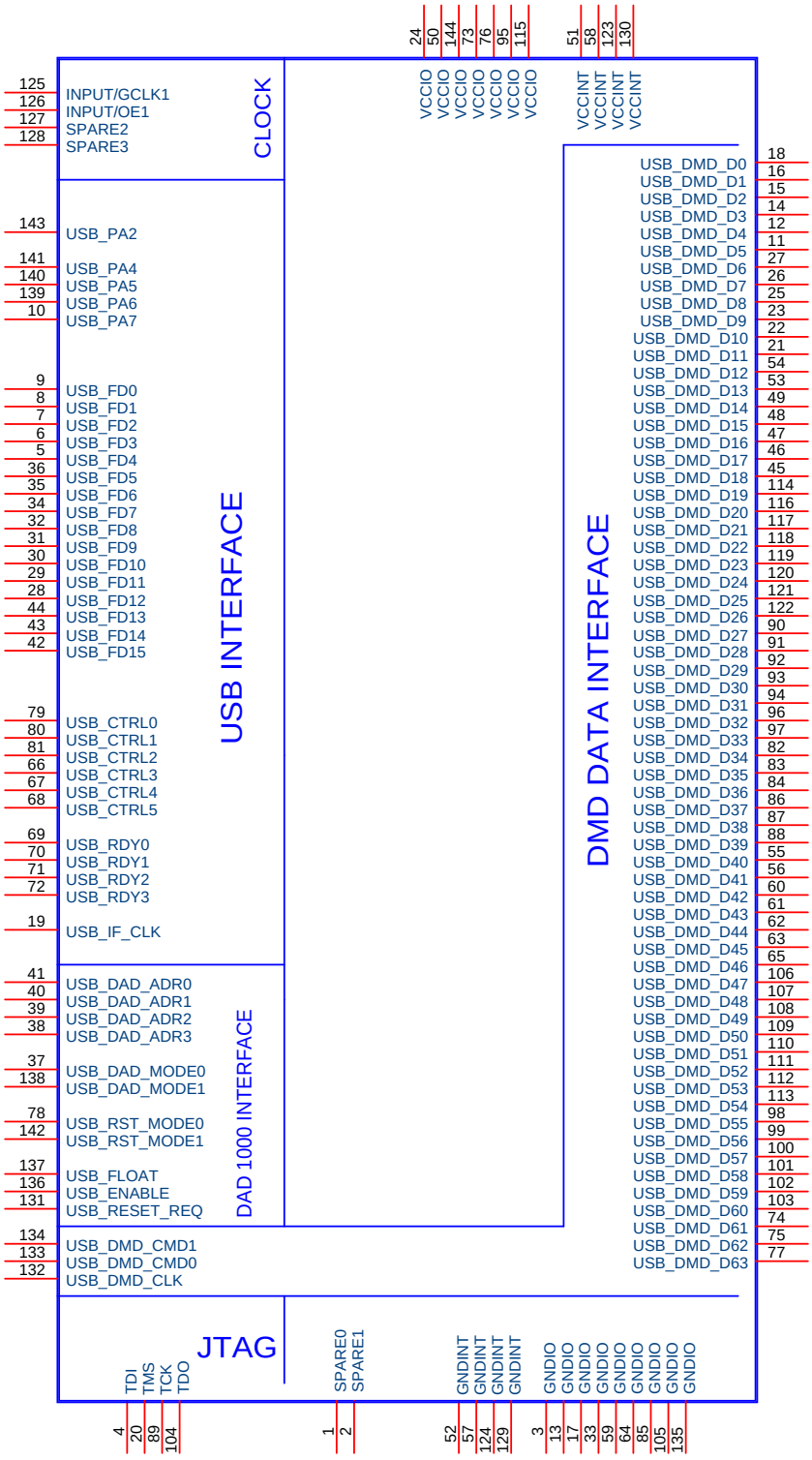

Figure 5 Part Schematic Symbol

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6 General Electrical Requirements

6.1 Absolute Maximum Rating

Table 4 Absolute Maximum Ratings					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage	With respect to ground	-0.5	3.6	V
V_{CCIO}	Supply voltage		-0.5	3.6	V
V_I	DC input voltage	*(1)*	-2.0	4.6	V
I_{OUT}	DC output current, per pin		-33	50	mA
T_{SIG}	Storage temperature	No bias	-65	150	° C
T_A	Ambient temperature	Under bias	-65	135	° C
T_J	Junction temperature	Under bias	-65	135	° C

6.2 Recommended Operating Conditions

Table 5 Recommended Operating Condition					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{CCINT}	Supply voltage for internal logic and input buffers		3.0	3.6	V
V_{CCIO}	Supply voltage for output drivers, 3.3-V operation		3.0	3.6	V
	Supply voltage for output drivers, 2.5-V operation		2.3	2.7	V
V_{CCISP}	Supply voltage during in-system programming		2.375	2.625	V
V_I	Input voltage	*(2)*	-0.5	3.9	V
V_O	Output voltage	Under bias	0	V_{CCIO}	V
T_A	Ambient temperature		0	55	° C
T_J	Junction temperature		0	65	° C
t_R	Input rise time			40	ns
t_F	Input fall time			40	ns

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6.3 Device DC Operating Conditions

Table 6 Device DC Operating Conditions					
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Unit**
V_{IH}	High-level input voltage		2.0	3.9	V
V_{IL}	Low-level input voltage		–0.5	0.8	V
V_{OH}	3.3-V high-level CMOS output voltage	I_{OH} = —0.1 mA DC, V_{CCIO} = 3.00 V ***(3)***	V_{CCIO} -0.2		V
V_{OL}	3.3-V low-level CMOS output voltage	I_{OL} = 0.1 mA DC, V_{CCIO} = 3.00 V ***(4)***		0.2	V
I_I	Input leakage current	V_I = -0.5 to 3.9 V ***(5)***	-10	10	µA
I_{OZ}	Tri-state output off-state current	V_I = -0.5 to 3.9 V ***(5)***	-10	10	µA

Notes to tables:

(1) Minimum DC input voltage is –0.5 V. During transitions, the inputs may undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

(2) All pins, including dedicated inputs, I/O pins, and JTAG pins, may be driven before VCCINT and VCCIO are powered.

(3) The parameter is measured with 50% of the outputs each sourcing the specified current. The I OH parameter refers to high-level TTL or CMOS output current.

(4) The parameter is measured with 50% of the outputs each sinking the specified current. The I OL parameter refers to low-level TTL or CMOS output current.

(5) This value is specified for normal device operation. The maximum leakage current during power-up is ±300 µA.

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7 USBIFC PIN MAP

Table 7 USBIFC Pin Map

NAME	I/O	DESCRPTION	Connect To	PIN #
SPARE0		Reserved	No Connect	1
SPARE1	O	Reserved	User Output	2
GND	P	GND	Ground	3
TDI	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	4
FD4	I	Data from USB chip with series termination	FX2 PIN 54	5
FD3	I	Data from USB chip with series termination	FX2 PIN 47	6
FD2	I	Data from USB chip with series termination	FX2 PIN 46	7
FD1	I	Data from USB chip with series termination	FX2 PIN 45	8
FD0	I	Data from USB chip with series termination	FX2 PIN 44	9
PA7	I	USB Control	FX2 PIN 92	10
USB_DMD_D5	O	Data to DMD with series termination	DMD PIN G3	11
USB_DMD_D4	O	Data to DMD with series termination	DMD PIN C1	12
GND	P	GND	Ground	13
USB_DMD_D3	O	Data to DMD with series termination	DMD PIN G1	13
USB_DMD_D2	O	Data to DMD with series termination	DMD PIN E5	15
USB_DMD_D1	O	Data to DMD with series termination	DMD PIN E3	16
GND	P	GND	Ground	17
USB_DMD_D0	O	Data to DMD with series termination	DMD PIN E1	18
USB_IF_CLK		Reserved	FX2 PIN 32	19
TMS	I	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	20
USB_DMD_D11	O	Data to DMD with series termination	DMD PIN H4	21
USB_DMD_D10	O	Data to DMD with series termination	DMD PIN A1	22
USB_DMD_D9	O	Data to DMD with series termination	DMD PIN H2	23
VCCIO1	P	VCC IO 3.3V	3.3 VOLT	24
USB_DMD_D8	O	Data to DMD with series termination	DMD PIN C3	25
USB_DMD_D7	O	Data to DMD with series termination	DMD PIN G7	26
USB_DMD_D6	O	Data to DMD with series termination	DMD PIN D4	27
FD12	I	Data from USB chip with series termination	FX2 PIN 121	28
FD11	I	Data from USB chip with series termination	FX2 PIN 105	29
FD10	I	Data from USB chip with series termination	FX2 PIN 104	30
FD9	I	Data from USB chip with series termination	FX2 PIN 103	31
FD8	I	Data from USB chip with series termination	FX2 PIN 102	32
GND	P	GND	Ground	33
FD7	I	Data from USB chip with series termination	FX2 PIN 57	34
FD6	I	Data from USB chip with series termination	FX2 PIN 56	35
FD5	I	Data from USB chip with series termination	FX2 PIN 55	36
USB_DAD_MODE0	O	USB DAD Mode Select	DRC PIN 10	37
USB_DAD_ADDR3	O	USB DAD Reset Block address select	DRC PIN 12	38
USB_DAD_ADDR2	O	USB DAD Reset Block address select	DRC PIN 13	39
USB_DAD_ADDR1	O	USB DAD Reset Block address select	DRC PIN 14	40
USB_DAD_ADDR0	O	USB DAD Reset Block address select	DRC PIN 92	41
FD15	O	Data to USB with series termination	FX2 PIN 124	42

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Table 7 USBIFC Pin Map

NAME	I/O	DESCRPTION	Connect To	PIN #
FD14	O	Data to USB with series termination	FX2 PIN 123	43
FD13	O	Data to USB with series termination	FX2 PIN 122	44
USB_DMD_D18	O	Data to DMD with series termination	DMD PIN B4	45
USB_DMD_D17	O	Data to DMD with series termination	DMD PIN K4	46
USB_DMD_D16	O	Data to DMD with series termination	DMD PIN B6	47
USB_DMD_D15	O	Data to DMD with series termination	DMD PIN K6	48
USB_DMD_D14	O	Data to DMD with series termination	DMD PIN D10	49
VCCIO1	P	VCC IO 3.3V	3.3 VOLT	50
VCCINT	P	VCC IO 2.5V	2.5 Volt	51
GND	P	GND	Ground	52
USB_DMD_D13	O	Data to DMD with series termination	DMD PIN H6	53
USB_DMD_D12	O	Data to DMD with series termination	DMD PIN D6	54
USB_DMD_D40	O	Data to DMD with series termination	DMD PIN A25	55
USB_DMD_D41	O	Data to DMD with series termination	DMD PIN C21	56
GND	P	GND	Ground	57
VCCINT	P	VCC IO 2.5V	2.5 Volt	58
GND	P	GND	Ground	59
USB_DMD_D42	O	Data to DMD with series termination	DMD PIN C25	60
USB_DMD_D43	O	Data to DMD with series termination	DMD PIN M26	61
USB_DMD_D44	O	Data to DMD with series termination	DMD PIN A27	62
USB_DMD_D45	O	Data to DMD with series termination	DMD PIN K28	63
GND	P	GND	Ground	64
USB_DMD_D46	O	Data to DMD with series termination	DMD PIN D22	65
CTRL3	I	USB Control Input	FX2 PIN 66	66
CTRL4	I	USB Control Input	FX2 PIN 67	67
CTRL5	I	USB Control Input	FX2 PIN 98	68
RDY0	O	USB Ready Output	FX2 PIN 4	69
RDY1	O	USB Ready Output	FX2 PIN 5	70
RDY2	O	USB Ready Output	FX2 PIN 6	71
RDY3	O	USB Ready Output	FX2 PIN 7	72
VCCIO2	P	VCC IO 3.3V	3.3 VOLT	73
USB_DMD_D61	O	Data to DMD with series termination	DMD PIN F30	74
USB_DMD_D62	O	Data to DMD with series termination	DMD PIN F28	75
VCCIO2	P	VCC IO 3.3V	3.3 VOLT	76
USB_DMD_D63	O	Data to DMD with series termination	DMD PIN F26	77
USB_RST_MODE0	O	FUTURE	DRC PIN 8	78
CTRL0	I	USB Control Input	FX2 PIN 69	79
CTRL1	I	USB Control Input	FX2 PIN 70	80
CTRL2	I	USB Control Input	FX2 PIN 71	81
USB_DMD_D34	O	Data to DMD with series termination	DMD PIN A19	82
USB_DMD_D35	O	Data to DMD with series termination	DMD PIN A21	83
USB_DMD_D36	O	Data to DMD with series termination	DMD PIN C19	84
GND	P	GND	Ground	85
USB_DMD_D37	O	Data to DMD with series termination	DMD PIN D18	86
USB_DMD_D38	O	Data to DMD with series termination	DMD PIN B22	87

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Table 7 USBIFC Pin Map

NAME	I/O	DESCRPTION	Connect To	PIN #
USB_DMD_D39	O	Data to DMD with series termination	DMD PIN B34	88
TCK	I	JTAG – Pull down with 1k ohm to ground.	See Note 1	89
USB_DMD_D27	O	Data to DMD with series termination	DMD PIN A9	90
USB_DMD_D28	O	Data to DMD with series termination	DMD PIN B12	91
USB_DMD_D29	O	Data to DMD with series termination	DMD PIN C13	92
USB_DMD_D30	O	Data to DMD with series termination	DMD PIN A13	93
USB_DMD_D31	O	Data to DMD with series termination	DMD PIN A15	94
VCCIO2	P	VCC IO 3.3V	3.3 VOLT	95
USB_DMD_D32	O	Data to DMD with series termination	DMD PIN D16	96
USB_DMD_D33	O	Data to DMD with series termination	DMD PIN B18	97
USB_DMD_D55	O	Data to DMD with series termination	DMD PIN J29	98
USB_DMD_D56	O	Data to DMD with series termination	DMD PIN D24	99
USB_DMD_D57	O	Data to DMD with series termination	DMD PIN G27	100
USB_DMD_D58	O	Data to DMD with series termination	DMD PIN D28	101
USB_DMD_D59	O	Data to DMD with series termination	DMD PIN G29	102
USB_DMD_D60	O	Data to DMD with series termination	DMD PIN D30	103
TDO	O	JTAG – Pull up with 1k ohm to 3.3V	See Note 1	104
GND	P	GND	Ground	105
USB_DMD_D47	O	Data to DMD with series termination	DMD PIN K26	106
USB_DMD_D48	O	Data to DMD with series termination	DMD PIN B30	107
USB_DMD_D49	O	Data to DMD with series termination	DMD PIN K30	108
USB_DMD_D50	O	Data to DMD with series termination	DMD PIN B28	109
USB_DMD_D51	O	Data to DMD with series termination	DMD PIN J25	110
USB_DMD_D52	O	Data to DMD with series termination	DMD PIN C27	111
USB_DMD_D53	O	Data to DMD with series termination	DMD PIN J27	112
USB_DMD_D54	O	Data to DMD with series termination	DMD PIN J27	113
USB_DMD_D19	O	Data to DMD with series termination	DMD PIN D26	114
VCCIO2	P	VCC IO 3.3V	3.3 VOLT	115
USB_DMD_D20	O	Data to DMD with series termination	DMD PIN C9	116
USB_DMD_D21	O	Data to DMD with series termination	DMD PIN L3	117
USB_DMD_D22	O	Data to DMD with series termination	DMD PIN C7	118
USB_DMD_D23	O	Data to DMD with series termination	DMD PIN A3	119
USB_DMD_D24	O	Data to DMD with series termination	DMD PIN A7	120
USB_DMD_D25	O	Data to DMD with series termination	DMD PIN D12	121
USB_DMD_D26	O	Data to DMD with series termination	DMD PIN B10	122
VCCINT	P	VCC IO 2.5V	2.5 Volt	123
GND	P	GND	Ground	124
60MHZ_CLK	I	RESERVED		125
OE2	I	RESERVED		126
GND	P	GND	Ground	127
GND	P	GND	Ground	128
GND	P	GND	Ground	129
VCCINT	P	VCC IO 2.5V	2.5 Volt	130
USB_RESET_REQ	O	DAD Reset Request	DRC PIN 36	131
USB_DMD_CLK	O	DMD DDR CLOCK	HSC PIN 2	132
USB_DMD_CMDO	O	DMD CONTROL	HSC PIN 5	133

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Table 7 USBIFC Pin Map				
NAME	**I/O**	**DESCRPTION**	**Connect To**	**PIN #**
USB_DMD_CMD1	O	DMD CONTROL	HSC PIN 6	134
GND	P	GND	Ground	135
USB_PORT_EN	O	USB Port Enable	DRC PIN 29	136
USB_FLOAT	O	USB Float Request	DRC PIN 37	137
USB_DAD_MODE1	O	USB DAD Mode Select	DRC PIN 9	138
PA6	I	USB Control	FX2 PIN 91	139
PA5	I	USB Port Enable	FX2 PIN 90	140
PA4	I	USB Control	FX2 PIN 89	141
USB_RST_MODE1		FUTURE	DRC PIN 7	142
PA2		USB Control	FX2 PIN 84	143
VCCIO1	P	VCC IO 3.3V	3.3 VOLT	144

Note 1. User may bring these signals to a connector for possible future use. The programmed contents of this device are protected from being changed or duplicated. Use of these signals to change the programmed contents of this device could damage the USBIFC and the DMD and void the warranty.

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8 ACRONYMS

DAD 1000 DMD Power and Reset Driver

DDR Double Data Rate

SDR Single Data Rate

DMD Digital Micromirror Device

GUI Graphical User Interface

USB Universal Serial Bus

DRC DAD Reset Controller

HSC High-speed Controller

USBIFC USB Interface Controller

SCP Serial Communications Port

CDS Customer Data Sheet

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